Vijayanand (Vijay) Nagarajan

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CURRENT APPOINTMENT

Professor, Kahlert School of Computing, University of Utah, July 2023 - present.

EDUCATION

Ph.D. in Computer Science, University of California Riverside, September 2009.

M.S. in Computer Science, The University of Arizona, May 2005.

B.E (Bachelor of Engineering) in Computer Science, University of Madras, March 2003.

PREVIOUS APPOINTMENTS

Personal Chair (Full Professor), School of Informatics, University of Edinburgh, August 2022 - present (On a leave of absence)

Reader (Associate Professor), School of Informatics, University of Edinburgh, August 2015 - July 2022.

Honorary Visiting Faculty, Department of CSE, IIT Madras, November 2018 - March 2019

Lecturer (Assistant Professor), School of Informatics, University of Edinburgh, October 2009 - July 2015.

Research Assistant, Dept. of Computer Science and Eng., UC Riverside, August 2007 - September 2009.

Research Intern, Programming Systems Lab, Intel Corporation, May 2006 - August 2006.

Research Assistant, Dept. of Computer Science., Univ of Arizona, May 2004 - July 2007.

AWARDS AND HONOURS

Intel 2013 Early Career Faculty Honour Award

IEEE MICRO Top Picks: "HeteroGen: Automatic Synthesis of Heterogeneous Cache Coherence Protocols," HPCA 2022.

IEEE MICRO Top Picks Honorable Mention: "Hermes: A Fast, Fault-Tolerant and Linearizable Replication Protocol," ASPLOS 2020.

IEEE MICRO Top Picks Honorable Mention: "ProtoGen: Automatically Generating Directory Cache Coherence Protocols from Atomic Specifications," ISCA 2018.

PACT Best Paper Award: "Efficient Sequential Consistency Using Conditional Fences", PACT 2010.

PPoPP Best Paper Candidate: "Kite: Efficient and Available Release Consistency for the Datacenter", PPoPP 2020.

PhD Supervisor of Nicolai Oswald, 2019 Google fellowship.

PhD Supervisor of Bharghava Rajaram, Intel 2012 Doctoral Student Honour Award.

RESEARCH INTERESTS

My research interests span: Computer Architecture, Programming Languages and Computer Systems, with a focus on: Memory Consistency Models and Cache Coherence Protocols.

GRANTS

I hold or have held grants in excess of £3.4 million. The grant amounts listed below correspond to the Edinburgh portions.

Huawei (PI) *Near Memory Transactions*, £156,282 , 9/2022-8/2024.

iCASE Industry (PI) *Cache Coherence on non-uniform cache architectures* , £29,628 , 9/2021-8/2025.

EPSRC (PI) *Dijkstra's Pipe: Timing-Secure Processors by Design* , £535,239 , 7/2021-6/2024.

EPSRC (PI) *C6: Correct-by-Construction Heterogeneous Coherence*, £608,565 , 6/2021-6/2024.

Huawei: (PI) *HeteroGen: Automatically Generating Heterogeneous Coherence Protocols*, £175,838, 2018-2021

Leverhulme (PI) *Host of Visiting Professor: Prof. Daniel Sorin*, £24,395 , 2017.

SICSA (PI) *Host of Distinguished Visiting Fellow: Prof. Daniel Sorin*, £6080 , 2017.

EPSRC (Edinburgh PI) *C3: Scalable and verified shared memory via Consistency-directed Cache Coherence*, £668,897 , 6/2015-6/2018.

Amazon AWS Research Education Grant (PI), *Towards Efficient and Scalable Causal Consistency* $5250, 6/2015-6/2016

EPSRC (Edinburgh PI) *ESP-SD: Error tolerant Stream Processing System Design*, £441,324 , 10/2014-9/2017.

EPSRC (Edinburgh PI) *Anyscale Applications*, £ 482,610 , 9/2013-8/2017.

Intel (co-PI) *Dapper: Database inspired persistent Memory*, £174,762, 9/2013 - 8/2016 (PI: Stratis Viglas)

Intel (PI) *Early Career Faculty Honour*, £21,381, 10/2013 - 9/2014.

UKIERI (co-PI) *Power efficient and high performance data prefetching techniques for multi core processors*, £8,873, 1/2012 - 6/2014 (PI: Murray Cole)

PhD Students (graduated)

I have graduated 10 PhD students (7 as principal supervisor and 3 as co-supervisor). It is worth noting that I have worked closely and co-authored papers with my co-supervised students. I have also supervised and graduated 3 RAs. My supervisees are successfully placed in blue-chip industrial research labs as well as academic faculty positions.

Bharghava Rajaram, 2014 (*Assistant Professor, Mahindra Ecole Centrale, India*).

Andrew McPherson (with M. Cintra), 2015 (*First: IBM Research; Current: Senior Data Scientist, Credit Suisse*).

Cheng-Chieh Huang, 2015 (*Software Engineer, Google*).

Marco Elver, 2016 (*Software Engineer, Google, Mountain View, CA*).

Saumay Dublish (with N.P. Topham), 2018 (*Synopsis, starting Sep 2018*).

Arpit Joshi, 2018 (*Researcher, Intel, Portland, OR*)

Vasilis Gavrielatos, 2021 (*Research Scientist, Huawei*)

Antonis Katsarakis (with B. Grot), 2021 (*Research Scientist, Huawei*)

Nicolai Oswald, 2023 (*Research Scientist, NVIDIA*)

Adarsh Patil, 2023

Post-docs (graduated)

Sukarn Agarwal, 2023, (*Assistant Professor, IIT Mandi)*

Rakesh Kumar, 2017 (*Associate Professor, Norwegian University of Science and Technology)*

Jose Cano Reyes, 2018 (*Assistant Professor, Glasgow University)*

Chris Banks, 2018 (*Research Scientist, Roslin Institute and School of Veterinary studies, Edinburgh)*

PhD Students (in progress)

Mahesh Dananjaya, expected 2023

An-Qi Zhang, expected 2026

Post-docs (in progress)

Andres Goens

Imogen Morris

INVITED PRESENTATIONS

Duke, "Sharing Knowledge on Sharing State", Virtual, January 2022.

EPFL, "Sharing Knowledge on Sharing State", Virtual, November 2021.

Purdue, " Sharing Knowledge on Sharing State", Virtual, Sep 2021.

Utah, " Sharing Knowledge on Sharing State", Virtual, Sep 2021.

Imperial, " Sharing Knowledge on Sharing State", Virtual, Sep 2021.

IISc Bangalore, " Semantics-directed Shared Memory", Bangalore, India, Feb 2019.

IIT Kanpur, " Semantics-directed Shared Memory", Kanpur, India, Feb 2019.

ARM Research Summit, "Cache Coherence Protocols are Notoriously ~~Hard~~ Easy", Cambridge, UK, September 2018.

IIT Madras, "Scaling: Up and Out", Chennai, India, December 2017.

Intel Research, "Semantics-directed Hardware Design for Shared Memory", Intel Research, Bangalore, December 2017.

Dagstuhl Seminar, "Architectural Support for Persistent Memory", Dagstuhl, November 2017.

ARM Research Summit, "Scaling: Up and Out", Cambridge, UK, September 2017.

University of Pennsylvania, "Semantics-directed Hardware Design for Shared Memory", Philadelphia , USA, December 2016.

HP Labs, "Efficient Architecture Support for Persistent Memory", Palo Alto , USA, December 2016.

Princeton University, "Semantics-directed Hardware Design for Shared Memory", Princeton , USA, December 2016.

ARM Research Summit, "Semantics-directed Hardware Design for Shared Memory", Cambridge, UK, September 2016.

Newcastle University, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Newcastle, UK, August 2016.

University of Michigan, Computer Architecture Reading Group, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Ann Arbor, USA, June 2016.

Rutgers University, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", New Brunswick, USA, June 2016.

Queen's University Belfast, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Belfast, UK, April 2016.

Chennai Mathematical Institute, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Chennai, India, December 2015.

IIT Madras, Dept. of CSE, "Efficient Persist Barriers for Multicores", Madras, India, December 2015.

Huawei Research, Santa Clara, "Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Santa Clara, USA, October 2015.

UPMARC Workshop of Memory Models, Uppsala, "TSO-CC: Consistency-directed Cache Coherence for TSO", Uppsala, Sweden, February 2015.

University of Glasgow, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Glasgow, UK, October 2014.

Imperial College, London, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", London, UK, October 2014.

IISc Bangalore, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Bangalore, India, December 2013.

Beihang University, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Beijing, China, November 2013.

Intel Research, Santa Clara, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Santa Clara, USA, June 2013.

Intel Research, Braunschweig, "Efficient Sequential Consistency without Aggressive Speculation", Braunschweig, Germany, May 2012.

University of Manchester, APT Talk, "Monitoring Parallel Programs for Performance and Reliability", Manchester, UK, March 2011.

IIT Madras, Dept. of CSE, "Monitoring Parallel Programs for Performance and Reliability", Madras, India, July 2010.

University of Edinburgh, NAIS Annual Meeting, "Monitoring Parallel Programs for Performance and Reliability", Edinburgh, UK, June 2010.

University of Cambridge, Hardware Discussion Series, "Enabling Runtime Monitoring on Multicores", Cambridge, UK, June 2010.

INVITED SHORT COURSE

UPMARC Summer School, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Uppsala, Sweden, June 2016.

Beihang University, Invited Short course on "Hardware support for Shared Memory", Beijing, China, November 2013.

IIT Madras, Dept. of CSE, Invited Distinguished Short course on "Hardware Support for Shared Memory", Madras, India, December 2012.

PhD Committee: External

Apostolos Kokolis (UIUC), 2022

Sheel Sindhu Manohar (IIT Guwhati), 2022

Abdullah Khalufa (Manchester), 2021

Cristian Urlea (Glasgow), 2020

Xiaowei Ren (UBC), 2020

Sudhanshu Shukla (IIT Kanpur), 2019

Albert Esteve Garcia (Polytechnic University of Valencia), 2017

Raghavendra K (IIT Madras), 2017

Robert Norton (University of Cambridge), 2015

Mohammad Ashraful Anam (University College London), 2014

Meredydd Luff (University of Cambridge), 2012

Demian Rosas Ham (University of Manchester), 2012

PhD Committee: Internal

Erik Tomusk, 2016

Kiran Chandramohan, 2016

Alexander Collins, 2015

Murali Krishna Emani, 2015

Karthik Thucanakkenpalayam Sundararajan, 2013

Oscar Almer, 2012

Damon Fenacci, 2012

Luis Fabricio Goes, 2011

Richard Bennett, 2011

Pedro Diaz, 2011

BOOKS

Synthesis V. Nagarajan, D. J. Sorin, M. D., Hill, and, D. A. Wood, "A Primer on Memory Consistency and Cache Coherence, Second Edition" *Synthesis Lectures on Computer Architecture, Morgan and Claypool*, Feb 2020.

JOURNAL PUBLICATIONS[1]

*Top Picks** N. Oswald, V. Nagarajan, D. Sorin, V. Gavrielatos, T. Olausson, and R. Carr "HeteroGen: Automatic Synthesis of Heterogeneous Cache Coherence Protocols," *IEEE MICRO Top Picks from 2022 Computer Architecture Conferences*, July 2023, to appear.

[1]Contributions with an asterisk denote my most significant ones.

AURO J. Cano, D. R. White, A. Bordallo, C. McCreesh, A. L. Michala, J. Singer, and V. Nagarajan, "Solving the Task Variant Allocation Problem in Distributed Robotics" *Springer Autonomous Robots*, April 2018.

TACO S. Dublish, V. Nagarajan, and N. Topham, "Cooperative Caching for GPUs," *ACM Transactions on Architecture and Code Optimization*, January 2017.

*TACO** A.J. McPherson, V. Nagarajan, S. Sarkar and M. Cintra, "Fence placement for legacy data-race-free programs via synchronization read detection," *ACM Transactions on Architecture and Code Optimization*, January 2016.

IJPP C. Lin, V. Nagarajan, and R. Gupta, "Efficient Sequential Consistency Using Conditional Fences," *International Journal of Parallel Programming*, Vol. 40, No. 1, pages 84-117, special issue of Best Papers from PACT 2010, Feb 2012.

SP&E V. Nagarajan, D. Jeffrey, R. Gupta, and N. Gupta, "A System for Debugging via Online Tracing and Dynamic Slicing," *Software - Practice and Experience*, 26 pages, published online, July, 2011.

TOPLAS D. Jeffrey, V. Nagarajan, R. Gupta, and N. Gupta, "Execution Suppression: An Automated Iterative Technique for Locating Memory Bugs," *ACM Transactions on Programming Languages and Systems*, Vol. 32, No. 5. Article No. 17, 36 pages, May 2010.

IJPP C. Tian, M. Feng, V. Nagarajan, and R. Gupta, "Speculative Parallelization of Sequential Loops on Multicores," *International Journal of Parallel Programming*, Vol. 37, No. 5, pages 508-535, October 2009.

SP&E C. Tian, V. Nagarajan, R. Gupta, and S.Tallam "Automated Dynamic Detection of Busy-Wait Synchronizations," *Software - Practice and Experience*, Vol. 39, No. 11, pages 942-972, August 2009.

Trans. HiPEAC V. Nagarajan, R. Gupta, and A.Krishnaswamy, "Compiler-Assisted Memory Encryption for Embedded Processors," *Transactions on High Performance Embedded Architectures and Compilers*, Vol. 2, No. 1, pages 23-44, Springer Verlag, 2009 (Invited Paper – special issue of selected papers from HiPEAC Conference).

SIGOPS V. Nagarajan, and R. Gupta, "Runtime Monitoring on Multicores via OASES," *ACM SIGOPS Operating Systems Review*, special issue on the interaction among the OS, Compilers, and Multicore Processors, Vol. 43, No. 2, pages 15-24, April 2009 (Invited Paper).

CONFERENCE PUBLICATIONS

DSN A. Patil, V. Nagarajan, N. Nikoleris and N. Oswald "Apta: Fault-tolerant object-granular CXL disaggregated memory for accelerating FaaS," *The 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks*, June 2023, to appear.

*PLDI** A. Goens, S. Chakraborty, S. Sarkar, S. Agarwal, N. Oswald and V. Nagarajan, "Compound Memory Models," *The 44th ACM SIGPLAN Conference on Programming Language Design and Implementation (conditionally accepted), to appear*

*HPCA** N. Oswald, V. Nagarajan, D. Sorin, V. Gavrielatos, T. Olausson, and R. Carr "HeteroGen: Automatic Synthesis of Heterogeneous Cache Coherence Protocols," *The 28th IEEE International Symposium on High-Performance Computer Architecture* **(Designated IEEE MICRO 2022 Top Picks)**

ATC	M. Bailleu, D. Giantsidi, V. Gavrielatos, V. Nagarajan, and P. Bhatotia "Avacado: A Secure In-Memory Distributed Storage System," *Usenix Annual Technical Conference*, July 2021.
*ISCA**	A. Patil, V. Nagarajan, R. Balasubramonian, and N. Oswald "Dve: Improving DRAM Reliability and Performance On-Demand with Coherent Replication," *The 48th International Symposium on Computer Architecture*, June 2021.
*EuroSys**	V. Gavrielatos, A. Katsarakis, and V. Nagarajan "Odyssey: The Impact of Modern Hardware on Strongly-Consistent Replication Protocols," *The European Conference on Computer Systems*, Jan 2021.
*ISCA**	N. Oswald, V. Nagarajan, D. Sorin "HieraGen: Automatically Generating Hierarchical Cache Coherence Protocols from Atomic Specifications," *The 47th International Symposium on Computer Architecture*, June 2020.
*ASPLOS**	A. Katsarakis, V. Gavrielatos, M.R.S. Katebzadeh, A. Joshi, A. Dragojevich, B. Grot and V. Nagarajan, "Hermes: A Fast, Fault-Tolerant and Linearizable Replication Protocol," *The 25th International Conference on Architectural Support for Programming Languages and Operating Systems*, April, 2020. **(Designated IEEE MICRO 2020 Top Picks Honourable Mention)**
ASPLOS	M. Dananjaya, V. Gavrielatos, and V.Nagarajan, "Lazy Release Persistency," *The 25th International Conference on Architectural Support for Programming Languages and Operating Systems*, April, 2020.
*PPoPP**	V. Gavrielatos, A. Katsarakis, V. Nagarajan, B. Grot, and A. Joshi, "Kite: Efficient and Available Release Consistency for the Datacenter," *The 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, Feb, 2020. **(One of the 5 best paper candidates.)**
HPCA	S. Dublish, V. Nagarajan, and N. Topham, "Poise : Balancing Thread-Level Parallelism and Memory System Performance in GPUs using Machine Learning," *25th IEEE International Symposium on High-Performance Computer Architecture*, Feb 2019.
*ISCA**	N. Oswald, V. Nagarajan, D. Sorin "ProtoGen: Automatically Generating Directory Cache Coherence Protocols from Atomic Specifications," *The 45th International Symposium on Computer Architecture*, June 2018. **(Designated IEEE MICRO 2018 Top Picks Honourable Mention)**
*ISCA**	A. Joshi, V. Nagarajan, M. Cintra, and S. Viglas "DHTM: Durable Hardware Transactional Memory ," *The 45th International Symposium on Computer Architecture*, June 2018.
*EuroSys**	V. Gavrielatos, A. Katsarakis, A. Joshi, N. Oswald, B. Grot, and V. Nagarajan , "Scale-Out ccNUMA: Exploiting Skew with Strongly Consistent Caching," *The 13th European Conference on Computer Systems*, April 2018.
*ASPLOS**	R. Kumar, B. Grot, and V. Nagarajan, "Blasting Through The Front-End Bottleneck with Shotgun," *The 23rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, March 2018.
DATE	M. Elver, C. J. Banks, P. Jackson, and V. Nagarajan, "VerC3: A Library for Explicit State Synthesis for Concurrent Systems," *Design, Automation and Test in Europe*, to appear, March 2018.
IROS	J. Cano, Y. Yang, B. Bodin, V. Nagarajan, and M. O. Boyle, "Automatic Parameter Tuning of Motion Planning Algorithms" *IEEE/RSJInternational Conference on Intelligent Robots and Systems*, 2018.

*FMCAD** C. J. Banks, M. Elver, R. Hoffmann, S. Sarkar, P. Jackson, and V. Nagarajan, "Verification of a lazy cache coherence protocol against a weak memory model," *The 17th Conference on Formal Methods in Computer-Aided Design, Oct 2017*, to appear, Oct. 2017.

ISPASS S. Dublish, V. Nagarajan, and N. Topham, "Evaluating and Mitigating Bandwidth Bottlenecks Across the Memory Hierarchy in GPUs," *IEEE International Symposium on Performance Analysis of Systems and Software*, April 2017.

*HPCA** A. Joshi, V. Nagarajan, S. Viglas and M. Cintra, "ATOM: Atomic Durability in Non-volatile Memory through Hardware Support for Logging ," *The 23rd IEEE Symposium on High Performance Computer Architecture*, Feb. 2017.

*HPCA** R. Kumar, C. Huang, B. Grot, and V. Nagarajan, "Boomerang: a Metadata-Free Architecture for Control Flow Delivery ," *The 23rd IEEE Symposium on High Performance Computer Architecture*, Feb. 2017.

*MICRO** C. Huang, R. Kumar, M. Elver, B. Grot, and V. Nagarajan "C3D: Mitigating NUMA Effects via Coherent DRAM Caches" *The 49th ACM/IEEE International Symposium on Microarchitecture*, Oct. 2016

*SC** C. Huang, V. Nagarajan and A. Joshi "DCA: a DRAM-cache-aware DRAM controller" *The IEEE/ACM International Conference for High Performance Computing, Networking, Storage and Analysis*, Nov. 2016.

IROS J. Cano, A. Bordallo, V. Nagarajan, S. Ramamoorthy, and S. Vijayakumar "Automatic Configuration of ROS Applications for near-optimal Performance" *IEEE/RSJ International Conference on Intelligent Robots and Systems*, 2016.

*RSS** J. Cano, D. White, A. Bordallo, C. McCreesh, P. Prosser, J. Singer and V. Nagarajan, "Task Variant Allocation in Distributed Robotics" *Robotics: Science and Systems*, Ann Arbor, USA, June 2016.

*HPCA** M. Elver, and V. Nagarajan, "McVerSi: A Test Generation Framework for Fast Memory Consistency Verification in Simulation" *The 22nd Symposium on High Performance Computer Architecture*, Barcelona, Spain, March 2016.

*MICRO** A. Joshi, V. Nagarajan, S. Viglas and M. Cintra, "Efficient Persist Barriers for Multicores," *IEEE/ACM 48th International Symposium on Microarchitecture*, to appear, Dec. 2015.

*PACT** M. Elver, and V. Nagarajan, "RC3: Consistency directed Cache Coherence for x86-64 with RC extensions" *The 24th International Conference on Parallel Architectures and Compilation Techniques*, San Francisco, USA, October 2015.

SAFECOMP G. Stefanakis, V. Nagarajan and M. Cintra, "Understanding the Effects of Data Corruption on Application Behavior Based on Data Charecterestics" *International Conference on Computer Safety, Reliability and Security* , Delft, Netherlands, September 2015.

ICAR J. Cano, E. Molinos, V. Nagarajan and S. Vijayakumar, "Dynamic process migration in heterogeneous ROS-based environments" *The 17th International Conference on Advanced Robotics* , Istanbul, Turkey, July 2015.

SC C. Lin, V. Nagarajan, and R. Gupta, "Fence Scoping," *The IEEE/ACM International Conference for High Performance Computing, Networking, Storage and Analysis*, New Orleans, Louisiana, November 2014.

ICCD C. Huang, and V. Nagarajan, "Increasing Cache Capacity via Critical-words-Only Cache" *The 32nd IEEE International Conference on Computer Design*, Seoul, Korea, October 2014.

*PACT** C. Huang, and V. Nagarajan, "ATCache: Reducing DRAM cache Latency via a Small SRAM Tag Cache" *The 23rd International Conference on Parallel Architectures and Compilation Techniques*, Edmonton, Canada, August 2014.

*HPCA** M. Elver, and V. Nagarajan, "TSO-CC: Consistency directed cache coherence for TSO" *The International Symposium on High-Performance Computer Architecture*, Orlando, Florida, February 2014.

*PLDI** B.Rajaram, V. Nagarajan, S. Sarkar, and M.Elver, "Fast RMWs for TSO: Semantics and Implementation," *ACM SIGPLAN Conference on Programming Language Design and Implementation*, Seattle, Washington, June 2013.

ICS C.Lin, V. Nagarajan, and R. Gupta, "Address-aware Fences," *27th International Conference on Supercomputing*, Eugene, Oregon, June 2013.

CF B.Rajaram, V. Nagarajan, A.J.McPherson, and M. Cintra, "SuperCoP: A General Correct and Performance-efficient Supervised Memory System," *ACM International Conference on Computing Frontiers*, May 2012.

*ASPLOS** C.Lin, V. Nagarajan, R. Gupta, and B.Rajaram, "Efficient Sequential Consistency via Conflict Ordering," *ACM 17th International Conference on Architectural Support for Programming Languages and Operating Systems*, London, UK, March 2012.

*PACT** C.Lin, V. Nagarajan, and R. Gupta, "Efficient Sequential Consistency Using Conditional Fences," *19th International Conference on Parallel Architectures and Compilation Techniques* , pages 295-306, Vienna, Austria, September 2010. **(Recipient of a Best Paper Award)**

ISMM V. Nagarajan, D.Jeffrey and R. Gupta, "Self-Recovery in Server Programs," *8th International Symposium on Memory Management*, pages 49-58, Dublin, Ireland, June 2009.

*ISCA** V. Nagarajan, and R. Gupta, "ECMon: Exposing Cache events for Monitoring," *ACM/IEEE 36th International Symposium on Computer Architecture*, pages 349-360, Austin, Texas, June 2009.

*VEE** V. Nagarajan, and R. Gupta, "Architectural Support for Shadow Memory in Multiprocessors," *ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments*, pages 1-10, Washington DC, March 2009.

*MICRO** C. Tian, M. Feng, V. Nagarajan, and R. Gupta, "Copy or Discard Execution Model For Speculative Parallelization On Multicores," *IEEE/ACM 41st International Symposium on Microarchitecture*, pages 330-341, Lake Como, Italy, Nov. 2008.

*ISSTA** C. Tian, V. Nagarajan, R. Gupta, and S. Tallam, "Dynamic Recognition of Synchronization Operations for Improved Data Race Detection," *SIGSOFT International Symposium on Software Testing and Analysis*, pages 143-154, Seattle, July 2008.

ICSM V. Nagarajan, D. Jeffrey, R. Gupta, and N. Gupta, "ONTRAC: A System for Efficient ONline TRACing for Debugging," *International Conference on Software Maintenance*, pages 445-454, Paris, September 2007.

ICSM V. Nagarajan, R. Gupta, X. Zhang, M. Madou, B. De Sutter, and K. De Bosschere, "Matching Control Flow of Program Versions," *International Conference on Software Maintenance*, pages 84-93, Paris, September 2007.

*HiPEAC** V.Nagarajan, R. Gupta, and A.Krishnaswamy, "Compiler-Assisted Memory Encryption for Embedded Processors," *International Conference on High Performance Embedded Architectures and Compilers*, Springer Verlag, LNCS 4367, pages 7-22, Ghent, Belgium, January 2007.

WORKSHOP PUBLICATIONS

LATTE	V. Nagarajan, D. J. Sorin and and N. Oswald, "Insights from the *Gen Project," *Workshop on Languages, Tools, and Techniques for Accelerator Design* , March 2023
PaPoC	V. Gavrielatos, V. Nagarajan, and P. Fatourou, "Towards the Synthesis of Coherence/Replication Protocols from Consistency Models via Real-Time Orderings.," *8th Workshop on Principles and Practice of Consistency for Distributed Data* , Jan 2021
NVMW	M. Cintra, A. Chatzistergiou, A. Joshi, V. Nagarajan, and S. Viglas, "Architectural Support for Atomic Durability in Non-Volatile Memory," *Non-Volatile Memories Workshop*, San Diego, USA, March 2018. (**Memorable Paper Award Finalist)**
NVMW	A. Joshi, V. Nagarajan, S. Viglas, and M. Cintra "DAPPER: a database-inspired approach to persistent memory," *Non-Volatile Memories Workshop*, San Diego, USA, March 2015.
LCPC	A. J. McPherson, V. Nagarajan, and M. Cintra, "Static Approximation of MPI Communication Graphs for Optimized Process Placement," *27th International Workshop on Languages and Compilers for Parallel Computing*, Hilsboro, USA, September 2014.
LCPC	V. Nagarajan and R. Gupta, "Speculative Optimizations for Parallel Programs on Multicores," *22nd International Workshop on Languages and Compilers for Parallel Computing*, Newark, Delaware, October 2009.
PADTAD	V. Nagarajan and R. Gupta, "Support for Symmetric Shadow Memory in Multiprocessors," *Workshop on Parallel and Distributed Systems: Testing, Analysis, and Debugging* (co-located with ISSTA), 9 pages, Seattle, July 2008.
NSFNGS	R. Gupta, N. Gupta, X. Zhang, D. Jeffrey, V. Nagarajan, S. Tallam and C. Tian, "Scalable Dynamic Information Flow Tracking and its Applications," *NSF Next Generation Software Workshop* (co-located with IPDPS), 5 pages, Florida, April 2008.
STMCS	C. Tian, V. Nagarajan, and R. Gupta, "Synchronization Aware Conflict Resolution for Runtime Monitoring Using Transactional Memory," *Workshop on Software Tools for Multicore Systems* (co-located with CGO), 6 pages, Boston, April 2008.
INTERACT	V. Nagarajan, H-S.Kim, Y.Wu and R. Gupta, "Dynamic Information Flow Tracking on Multicores," *Workshop on Interaction between Compilers and Computer Architectures* (co-located with HPCA), 10 pages, Salt Lake City, Feb. 2008.

TEACHING EXPERIENCE

I have taught Parallel Architectures (PA) and co-taught Computer Architecture (CAR). Over the years I have transformed the Parallel Architecture course with new material on GPUs and Transactional memory and new coursework on cache protocols; PA has turned out to be a critical course that several students on the Center for Doctoral training on Pervasive Parallelism take. Course feedback for both PA and CAR has been positive. **I was nominated for a EUSA teaching award in 2017/18 and 2022/23.** I also helped in integrating the separate computer design and computer architecture courses into the computer architecture and design course.

I was an MSc project coordinator during 2017-18 and was specifically responsible for addressing a critical problem: the system at that point could not handle the increased number of students, and the skew in the students' choices meant that a number of students were left without a project. I lead the specification of the new project portal interface, DPMT, its workflow, and managed its testing, thereby enabling DPMT to manage projects. **DPMT has since been used for both MSc and UG4 projects.**

CS4/MSc PA: Parallel Architectures: 2012/13, 2013/14, 2014/15, 2015/16, 2016/17, 2017/18, 2019/20, 2020/21, 2021/22

INF3 CARD: Computer Architecture and Design: 2019/20

INF3 CAR: Computer Architecture: 2011/12, 2012/13 (with Prof. Nigel Topham), 2013/14, 2014/15, 2015/16, 2016/17, 2017/18 (with Dr. Boris Grot)

iSLI : Microprocessors and Microcontrollers 2009/10

External teaching contributions. I am the lead author of the definitive textbook in my area, A Primer on Memory Consistency and Cache Coherence, 2nd edition, Morgan Claypool. **The book has been referred to as seminal by the ACM special interest group in computer architecture**. It has been downloaded more than 15000 times (the 6th most downloaded across all of the synthesis lecture series spanning computer science and beyond) and used in multiple universities including Duke and LMU Germany. I campaigned for the book to be made freely available, and thanks to the generosity of my co-authors and publishers, it is now free and has reached out to a large community of computer systems practitioners.

In addition to my teaching at Edinburgh, I've delivered the following invited short courses.

UPMARC Summer School, "Hardware Support for Shared-memory Concurrency: Reconciling Programmability with Performance", Uppsala, Sweden, June 2016.

Beihang University, Invited Short course on "Hardware support for Shared Memory", Beijing, China, November 2013.

IIT Madras, Dept. of CSE, Invited Distinguished Short course on "Hardware Support for Shared Memory", Madras, India, December 2012.

MASTERS AND UNDERGRADUATE STUDENTS

Jack Edgar, Bachelor project, 2022

Petr Vesely, MInf, 2022 *Distinction*

Carr Reece, Bachelor project, 2021 *Distinction and Prize*.

Theo Olausson, MInf, 2021 *Distinction and Prize*.

Ching Ling Yeung, Bachelor project, 2021

Jiawei Gu, Masters Project, 2020

Alex Wilson, Bachelor project, 2018, *Distinction*

Ahsen Tahir, MPhil, 2017

Georgios Stefanakis, MPhil, 2015

Scott Murray, Masters Project, 2014, *Distinction and Prize*.

Vinu Shankar Gopalan, Masters Project, 2012, *Distinction*.

Christian Lalanne, Masters project, 2012, *Distinction*.

Romil Lehakra, Masters Project, 2011

Ross Hamilton, Bachelors Project), 2011, *Distinction*.

CONTRIBUTIONS TO KNOWLEDGE EXCHANGE AND IMPACT

I have had significant collaboration with industry including with Intel, ARM and Huawei. I have had one patent with Intel and two others.

Our correct-by-construction coherence framework has already been used by Thales/IIT Madras for their safety-critical processor, and we are working with Huawei to integrate it into their tool flow via the HeteroGen project.

I collaborated with Intel on a 3-year URO funded project on persistent memory. Persistent memory is the new disruptive technology that has the potential to unify memory and storage. In collaboration with Intel, we proposed microarchitectural implementations of three such primitives: an ordering primitive (MICRO'15), atomic durability primitive (HPCA'17) and ACID transaction primitive (ISCA'18). We disclosed our findings to Intel in April 2016 suggesting an implementation in which the memory controller is logically persistent. Intel released an open disclosure consistent with our findings in Sep 2016 (deprecation of pcommit instruction).

I was invited into the the RISC-V memory model working group, tasked with designing the memory consistency model. RISC-V is a community effort for an open ISA and its associated ecosystem. This has generated huge interest both in industry as well as academia as a potential game-changer that can lead to computer architecture start-ups. Unfortunately, the original RISC-V memory model specification had bugs that rendered it inadequate to generate high-level language mappings. Consequently, a memory model task group was formed consisting of semantics, computer architecture and verification experts on memory models from the academia and industry. My research on consistency and cache coherence was discussed during the task group meetings. In particular, my work on atomicity semantics of a read-modify-writes [PLDI'13] helped the group arrive at a suitable atomicity semantics for RISC-V. Secondly, there was a technical debate on whether the RISC-V memory model should be TSO or any weaker. As part of the debate, my work and its follow-on works on non-speculative consistency enforcement were discussed. The memory model we co-designed has been recently ratified by the community and by the board of directors of the RISC-V foundation. It is worth noting that the utility of open and formal specification of memory model in this fashion goes beyond RISC-V as it serves as an exemplar for other companies to follow.

PROFESSIONAL ACTIVITIES

Associate Editor: IEEE Computer Architecture Letters (2019-2021)

General Chair: ACM LCTES 2017

Publicity Co-Chair: PPoPP 2020

Workshop Co-organizer: WAMS 2018

Finance Chair: PLDI 2014

Registration Chair: PACT 2013

Programme Committee Member: PPoPP 2023, HPCA 2023, PLDI 2022, HPCA 2021 (ERC), MICRO 2021 (ERC), ISCA 2021 (ERC), ISCA 2020, MICRO 2020 (ERC), MICRO 2019, HPCA 2019/2017, ASPLOS 2019 (ERC), CC 2018, SC 2016, ICCD 2015/2014, RTCSA 2016/2015/2014, NVMSA 2017/2016/2015, NAS 2015/2014, WODA 2014, MeAOW 2014, PACT 2018/2014 (ERC), PLDI 2014 (ERC), ICS 2014 (ERC), ASPLOS Doctoral Workshop 2012 (Mentor).

Past Steering Committee Member: LCTES, Numerical Algorithms and Intelligent Software (NAIS)

Past Member: RISC-V Memory Model Task group

Reviewer: NSERC Canada (grant reviewer), EPSRC (grant reviewer), ACM PLDI, ACM TACO, IEEE TC, JPDC, IEEE HPCA, IEEE TSC, ACM CF

ADMINISTRATIVE ACTIVITIES

Director of Institute for Computing Systems Architecture

Director of Equality, Diversity and Inclusion, August 2020-present I lead the School of Informatics "Decolonizing the Curriculum" effort, making Informatics courses inclusive, one of the first schools in the university to undertake this effort. I led a working group to understand what decolonization meant for Informatics, and the working group conducted workshops with each of the institutes to come to a shared understanding. We then asked each of the course organizers to come up with a list of actions

they are taking to making their course inclusive, and 90% of the 2020/21 courses have responded. The work we have done is listed as a case study at the University's "Decolonizing the Curriculum" hub.

I also led the development of the seminar/meeting organiser guidelines document for ensuring everybody is heard in meetings. I have several other initiatives in flight including: a proposal with the communications team for increasing the number and diversity of people who come forward with success stories, and a plan for disseminating EDI activities to the students.

MSc Convenor, 2019/20, I helped implement the no-detriment policy for MSc courses on the back of Covid.

Masters Project Coordinator, 2016/17, Led the specification, the backend workflow and the testing of the new DPMT project portal, which is now successfully used by both MSc and Honours projects.

UG4 Personal Tutor, 2014/15, 2015/16, 2016/17

UG3 Course Organiser, 2012/13, 2013/14, 2014/15, 2015/16

PhD Selection Committee, ICSA, 2011-2013

Seminar Organiser, ICSA, 2011-2013