

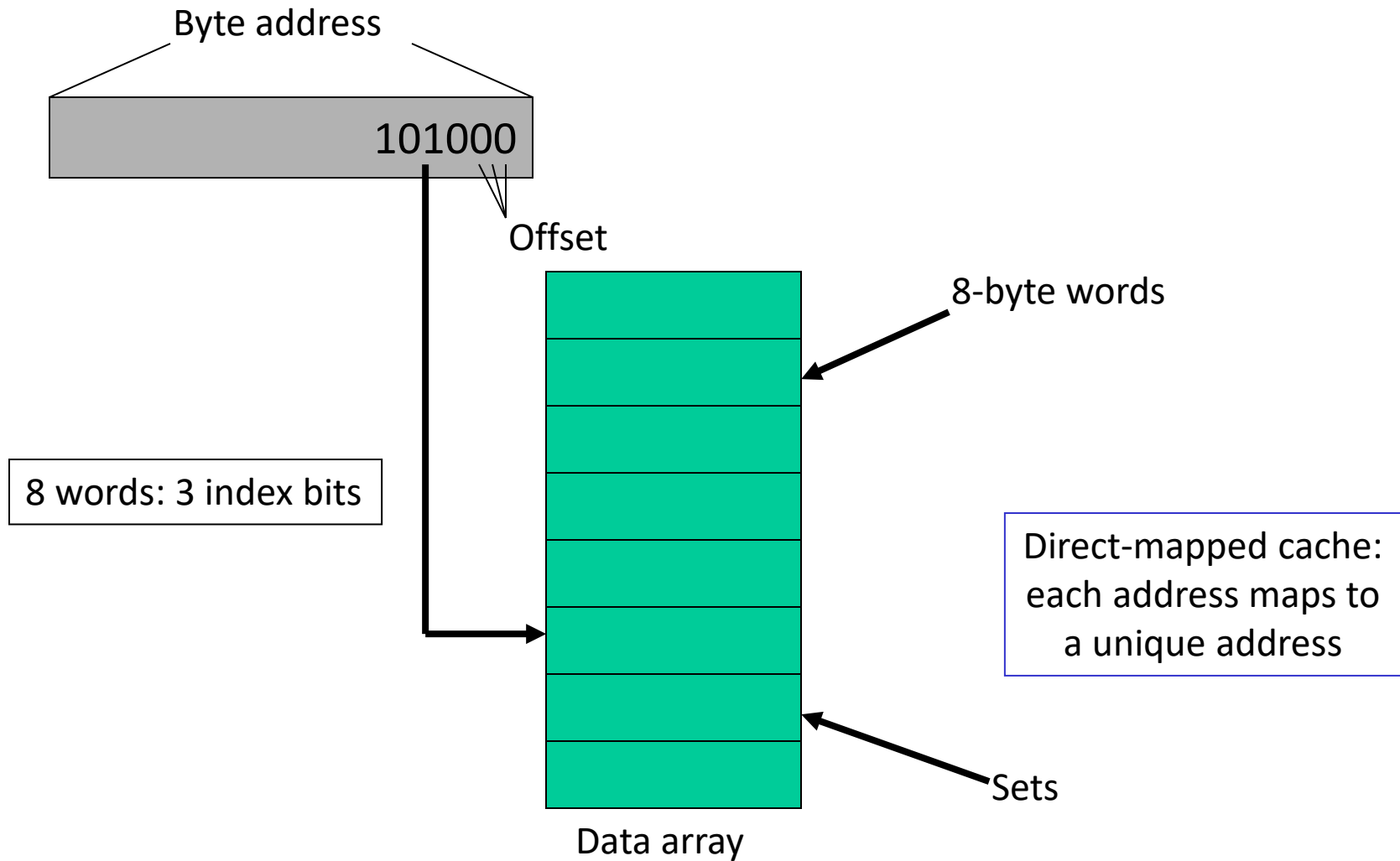
# Lecture: Cache Hierarchies

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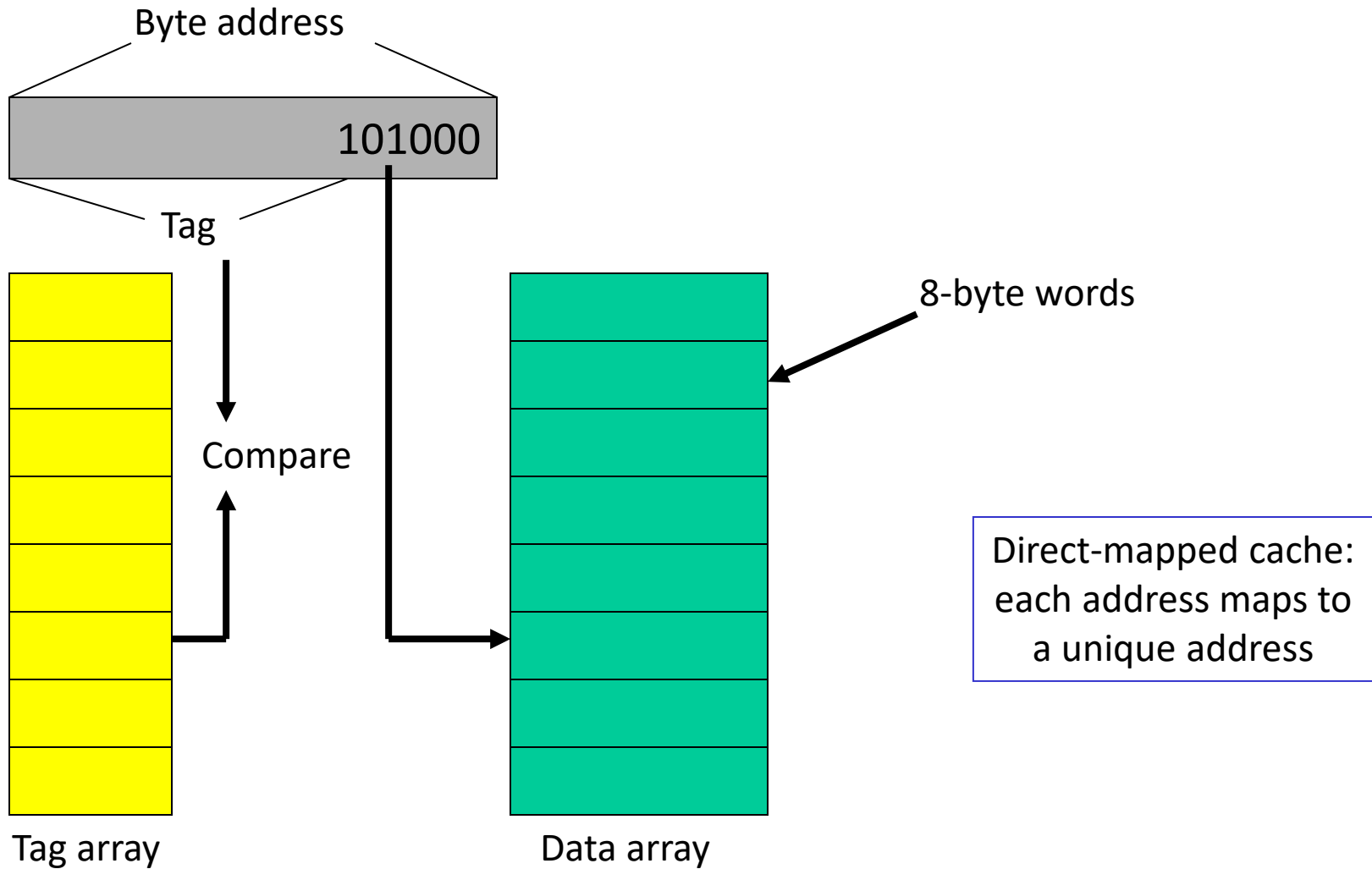
- Topics: cache access basics, example problems on cache access



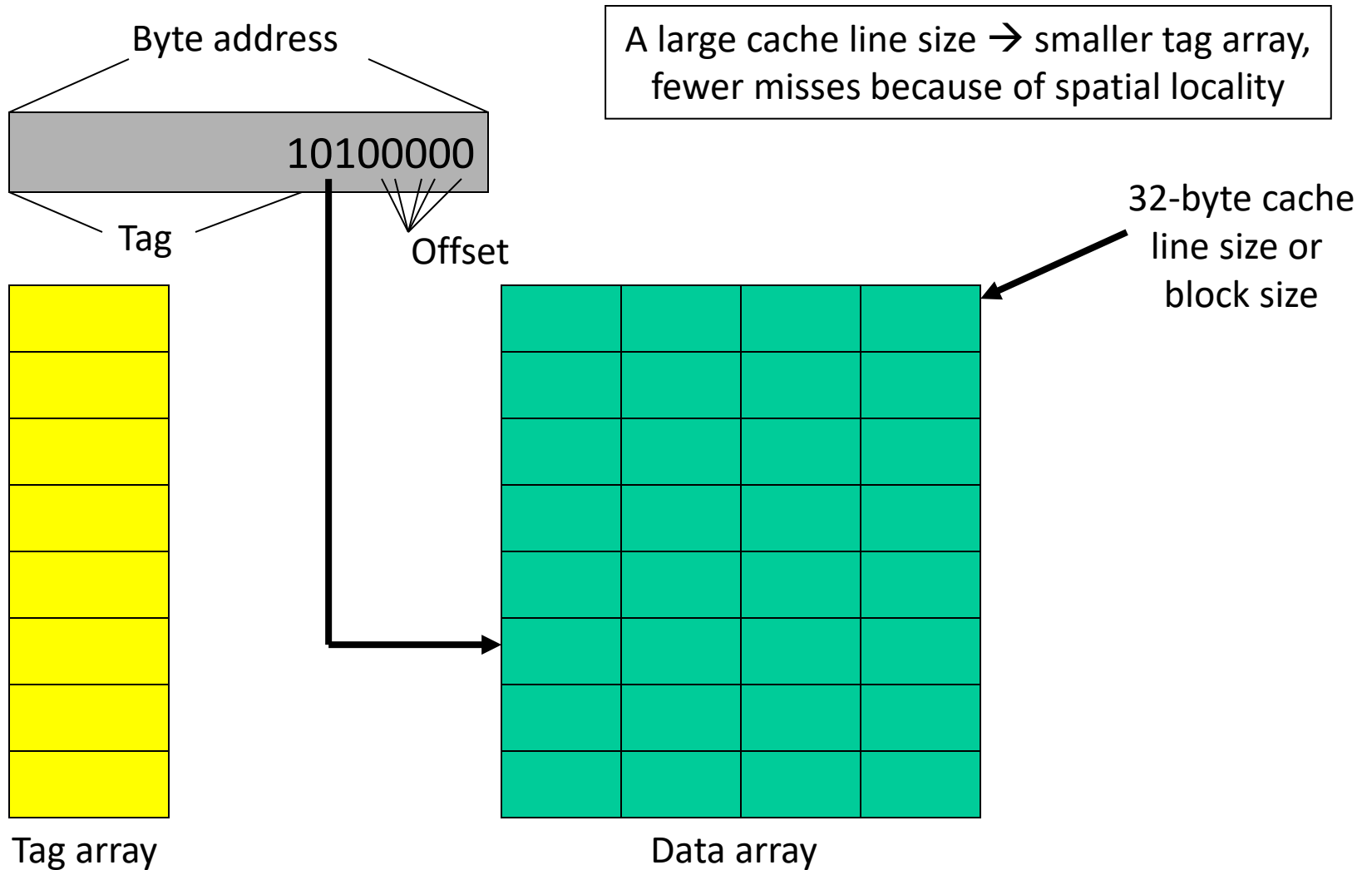
# Accessing the Cache



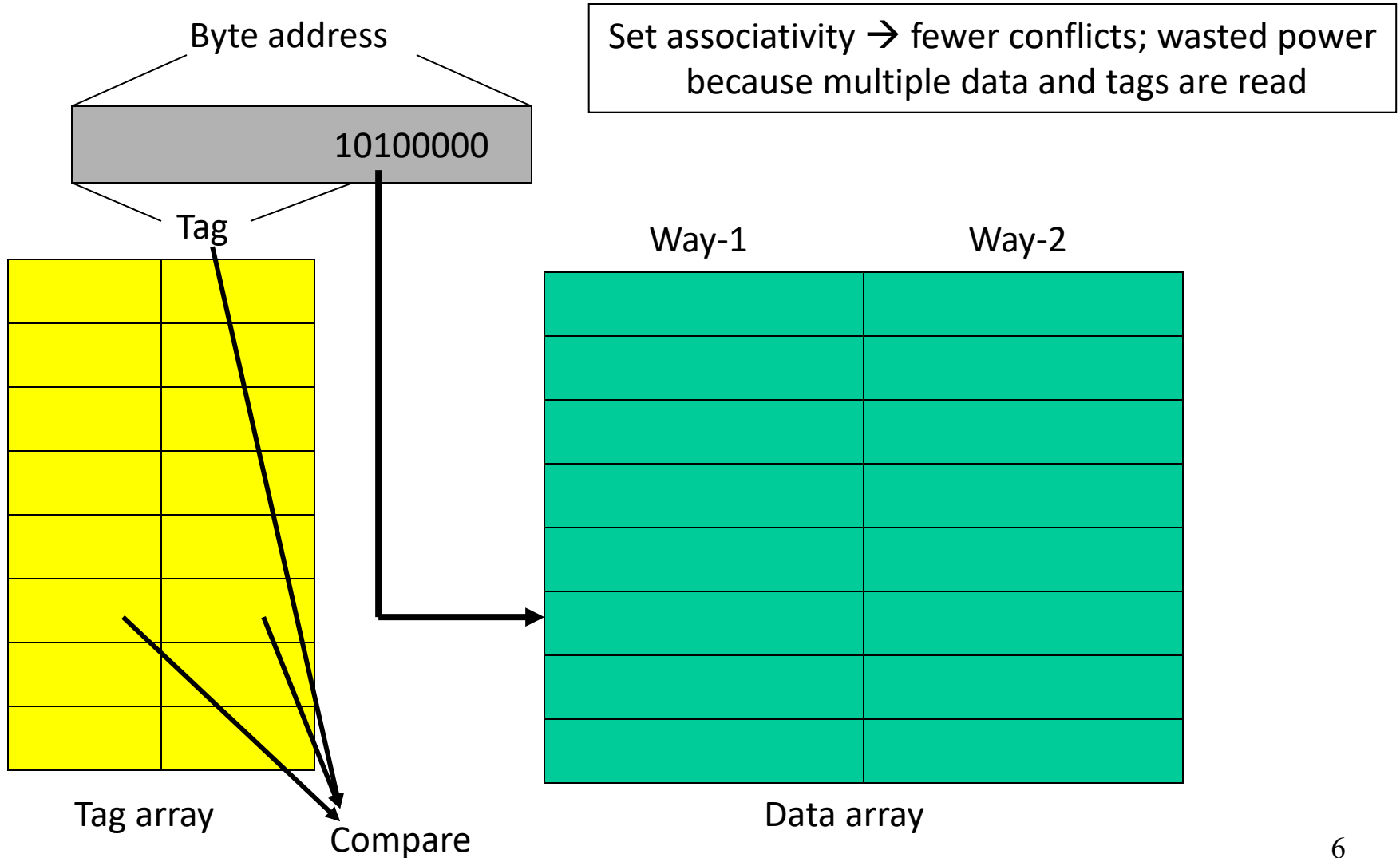
# The Tag Array



# Increasing Line Size



# Associativity



## Problem 2

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- Assume a direct-mapped cache with just 4 sets. Assume that block A maps to set 0, B to 1, C to 2, D to 3, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A

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A B B E C C A D B F A E G C G A

M M H M M H M M H M M M M M M



## Problem 3

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- Assume a 2-way set-associative cache with just 2 sets. Assume that block A maps to set 0, B to 1, C to 0, D to 1, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A

## Problem 3

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A B B E C C A D B F A E G C G A

M M H M M H M M H M H M M M H M

## Problem 4

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- 64 KB 16-way set-associative data cache array with 64 byte line sizes, assume a 40-bit address
- How many sets?
- How many index bits, offset bits, tag bits?
- How large is the tag array?

Equations:

Data array size (cache size) = #sets x #ways x blocksize

Tag array size = #sets x #ways x tagsize

Index bits =  $\log_2$  (#sets)

Offset bits =  $\log_2$  (blocksize)

Tag bits + index bits + offset bits = address width

# Problem 4

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- 64 KB 16-way set-associative data cache array with 64 byte line sizes, assume a 40-bit address
- How many sets? 64
- How many index bits (6), offset bits (6), tag bits (28)?
- How large is the tag array (28 Kb)?

# Problem 5

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- 8 KB fully-associative data cache array with 64 byte line sizes, assume a 40-bit address
- How many sets? How many ways?
- How many index bits, offset bits, tag bits?
- How large is the tag array?

# Problem 5

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- 8 KB fully-associative data cache array with 64 byte line sizes, assume a 40-bit address
- How many sets (1) ? How many ways (128) ?
- How many index bits (0), offset bits (6), tag bits (34) ?
- How large is the tag array (544 bytes) ?

Equations:

Data array size (cache size) = #sets x #ways x blocksize

Tag array size = #sets x #ways x tagsize

Index bits =  $\log_2$  (#sets)

Offset bits =  $\log_2$  (blocksize)

Tag bits + index bits + offset bits = address width

