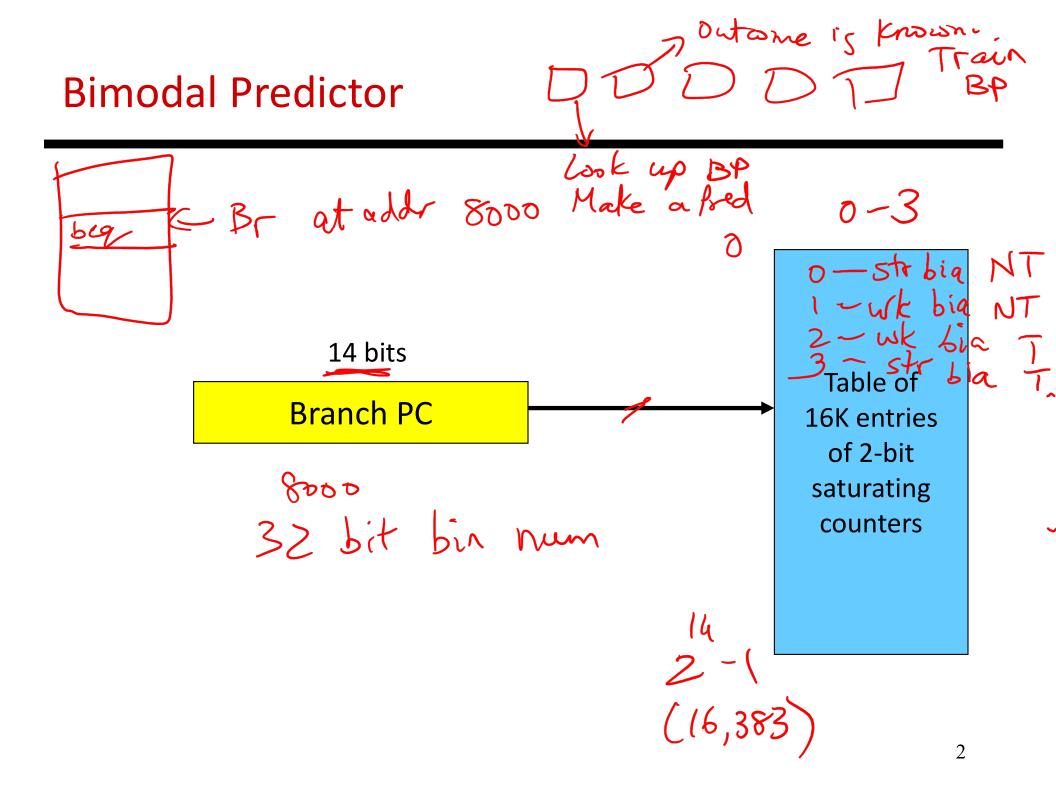


- Today's topics:
 - Branch Predictors
 - Out-of-order execution
- Midterm 2 next Tuesday
 - Same rules as for Midterm 1
 - Notes: bring the sheet from Midterm 1, a new sheet,
 plus the green sheet



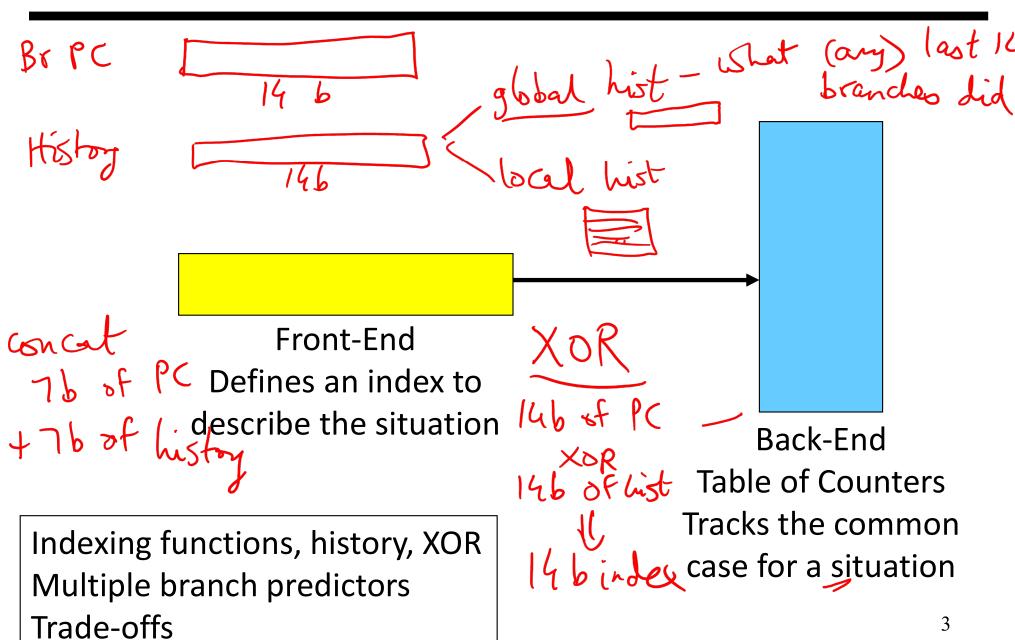
- Basic calculator, no phones/connectivity
- Content: starts at slide 7 lecture 8 (numerical reps)
 ends at slide 7 lecture 20 (out of order procs)

HW 5-8



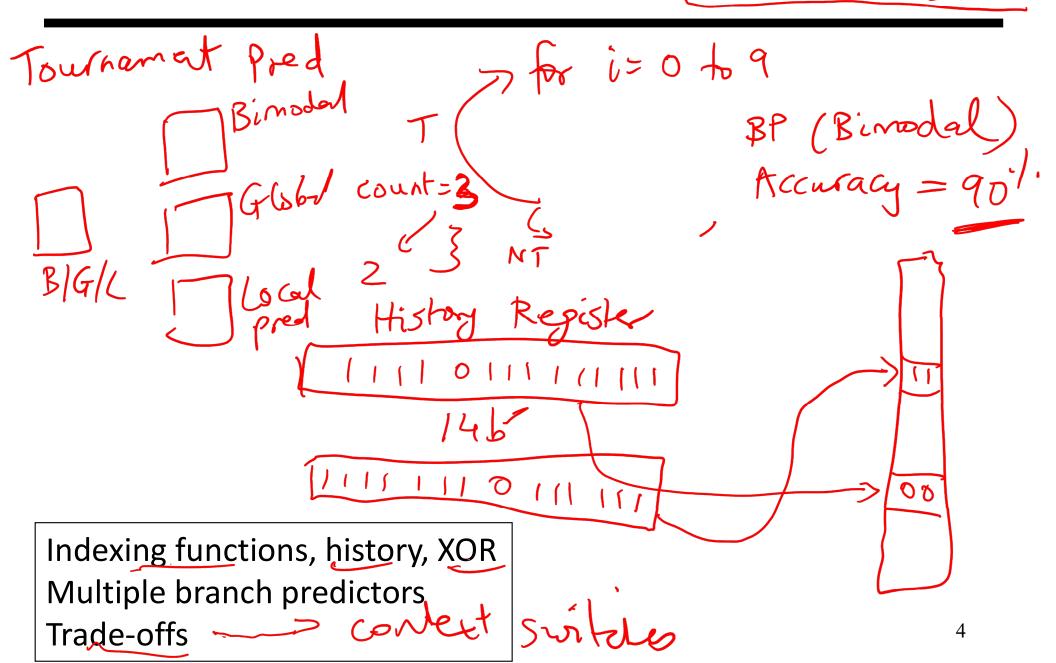
Advanced Predictors

1 XOR 0 => 1 XOR Odd 1's



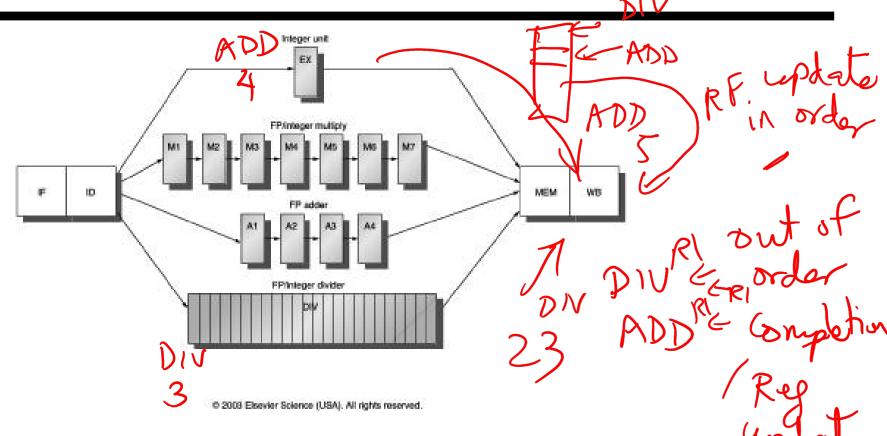
Advanced Predictors

Br Direction fred Br Target Pred BTB



Multicycle Instructions

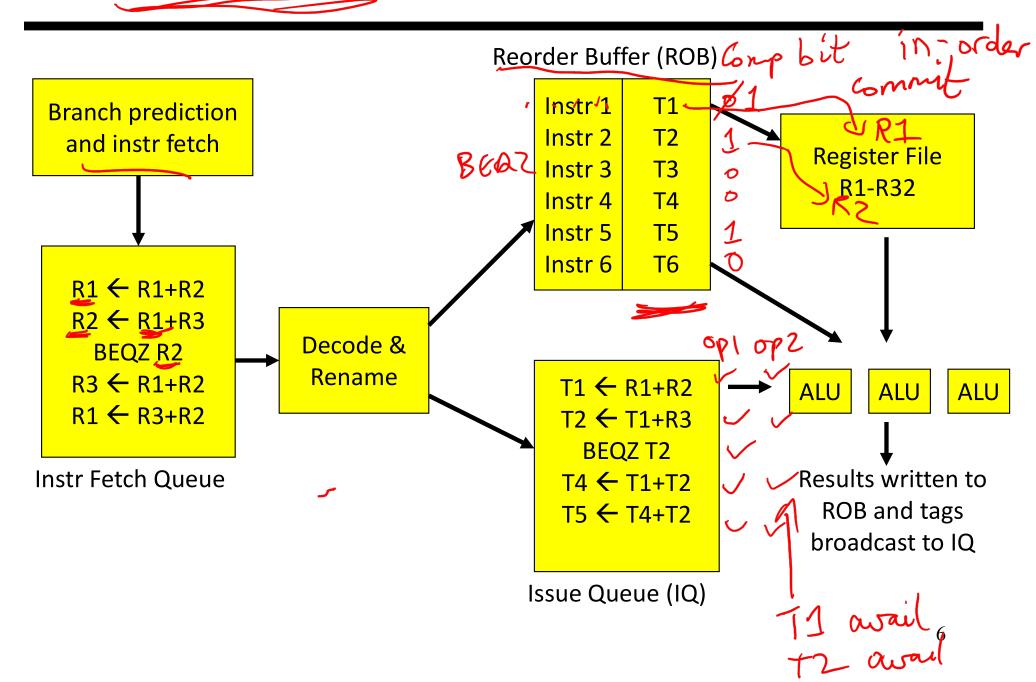
In order pipeline



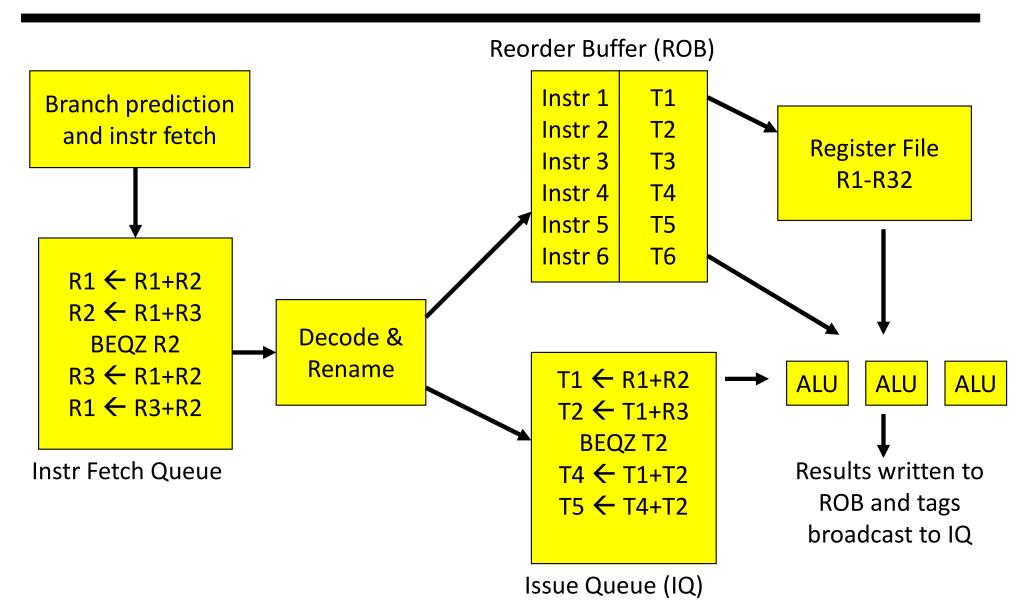
 Multiple parallel pipelines – each pipeline can have a different number of stages

 Instructions can now complete out of order – must make sure that writes to a register happen in the correct order

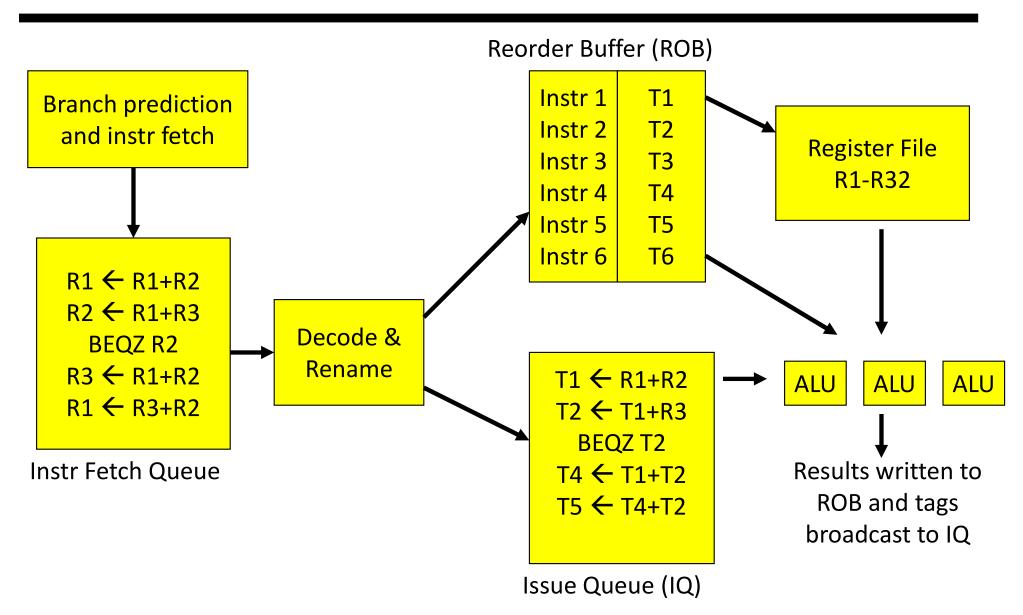
An Out-of-Order Processor Implementation



An Out-of-Order Processor Implementation



An Out-of-Order Processor Implementation



Example Code

Completion times

ADD R1, R2, R3

🗾 ADD R4, R1, R2

LW R5, 8(R4)

ADD R7, R6, R5

ADD R8, R7, R5

LW R9, 16(R4)

ADD R10, R6, R9

ADD R11, R10, R9

with in-order with ooo

Memory Hierarchy

As you go further, capacity and latency increase

Registers 1KB 1 cycle L1 data or instruction Cache 32KB 2 cycles

L2 cache 2MB 15 cycles Memory 16GB 300 cycles

Disk 1 TB 10M cycles