

Lecture 12: Hardware for Arithmetic

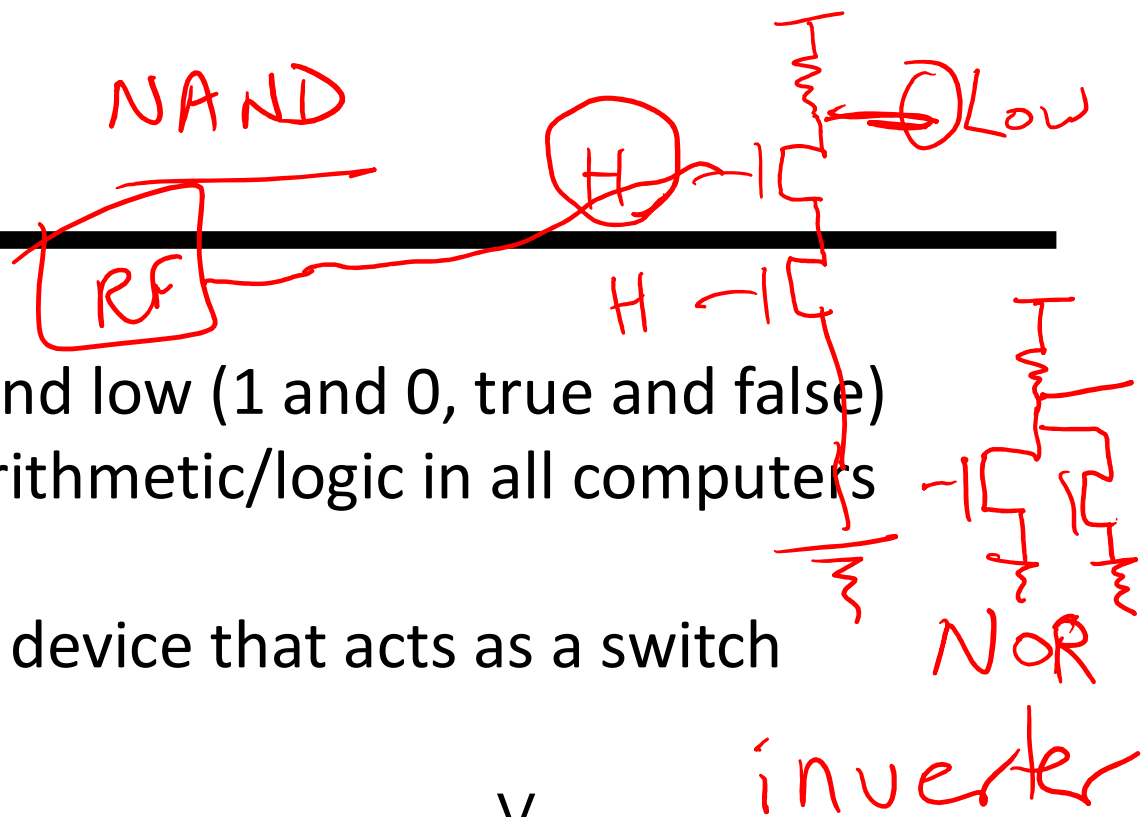
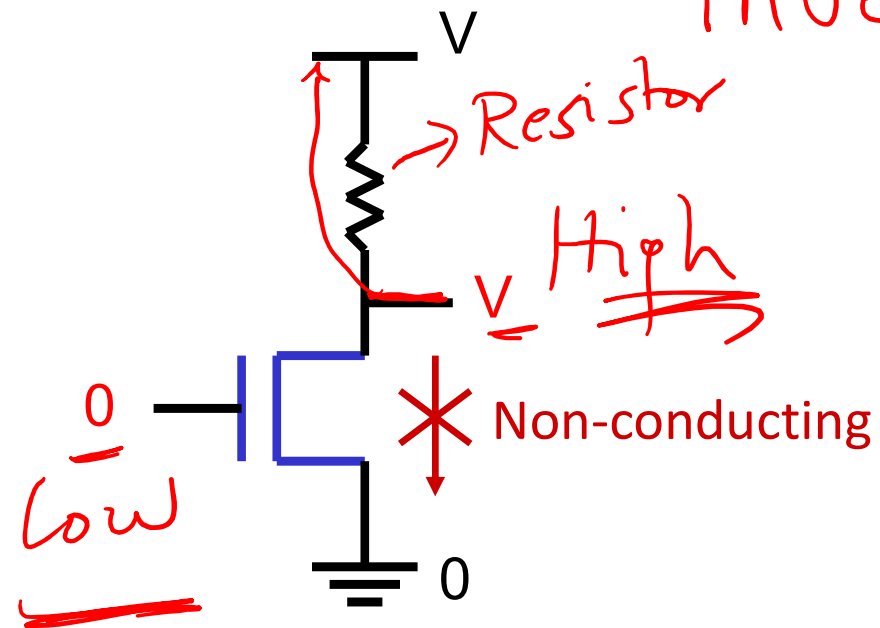
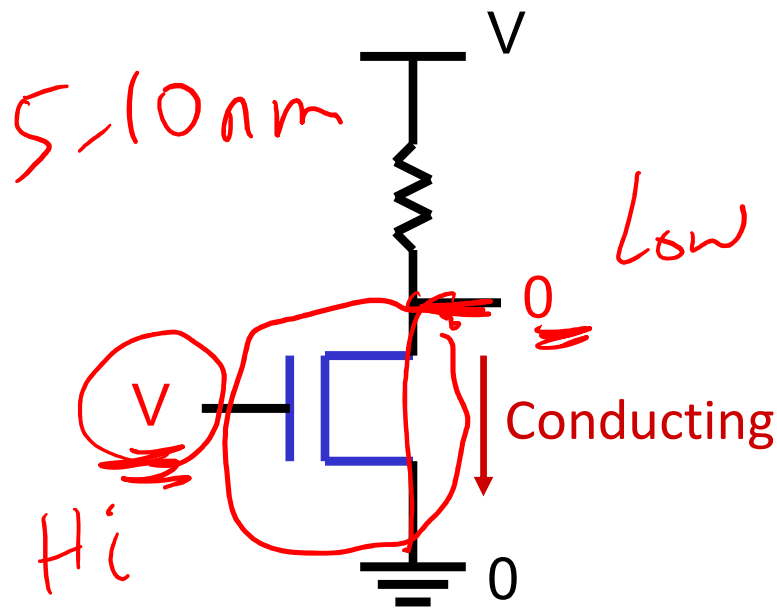
- Today's topics:
 - Digital logic intro
 - Logic for common operations
 - Designing an ALU

HW 4 due Friday

HW5 posted
later today.
Due in a week

Digital Design Basics

- Two voltage levels – high and low (1 and 0, true and false)
Hence, the use of binary arithmetic/logic in all computers
- A transistor is a 3-terminal device that acts as a switch



Logic Blocks

- A logic block has a number of binary inputs and produces a number of binary outputs – the simplest logic block is composed of a few transistors
- A logic block is termed combinational if the output is only a function of the inputs → memory-less ccts
- A logic block is termed sequential if the block has some internal memory (state) that also influences the output
- A basic logic block is termed a gate (AND, OR, NOT, etc.)

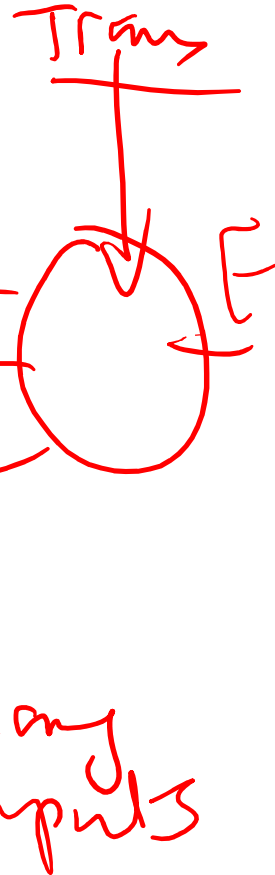
We will only deal with combinational circuits today

Truth Table

- A truth table defines the outputs of a logic block for each set of inputs

- Consider a block with 3 inputs A, B, C and an output E that is true only if *exactly* 2 inputs are true

A	B	C	E
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



Truth Table

- A truth table defines the outputs of a logic block for each set of inputs
- Consider a block with 3 inputs A, B, C and an output E that is true only if *exactly* 2 inputs are true

A	B	C	E
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Can be compressed by only representing cases that have an output of 1

Boolean Algebra

$+$ \cdot $-$
 \cup \cap $\neg A$

- Equations involving two values and three primary operators:

- OR : symbol $+$, $X = A + B \Rightarrow$ X is true if at least one of A or B is true

- AND : symbol \cdot , $X = A \cdot B \Rightarrow$ X is true if both A and B are true

- NOT : symbol $-$, $X = \bar{A} \Rightarrow$ X is the inverted value of A

Boolean Algebra Rules

- Identity law : $A + 0 = A$; $A \cdot 1 = A$
- Zero and One laws : $A + 1 = 1$; $A \cdot 0 = 0$
- Inverse laws : $A \cdot \bar{A} = 0$; $A + \bar{A} = 1$
- Commutative laws : $A + B = B + A$; $A \cdot B = B \cdot A$
- Associative laws : $A + (B + C) = (A + B) + C$
 $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- Distributive laws : $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$
 $A + (B \cdot C) = (A + B) \cdot (A + C)$

A handwritten example of the distributive law using arithmetic. It shows the calculation $7 \times (4 + 3)$ and its equivalent $(7 \times 4) + (7 \times 3)$. Red arrows point from the two distributive laws in the list above to this example. The first arrow points from $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ to the first part of the example, and the second arrow points from $A + (B \cdot C) = (A + B) \cdot (A + C)$ to the second part of the example.

$$7 \times (4 + 3) = (7 \times 4) + (7 \times 3)$$

DeMorgan's Laws

- $\overline{A + B} = \overline{A} \cdot \overline{B}$

Inverse
Negation of OR = AND of
inverses

- $\overline{A \cdot B} = \overline{A} + \overline{B}$

- Confirm that these are indeed true

Pictorial Representations

$$\overline{\overline{A}} \cdot \overline{\overline{B}}$$

AND



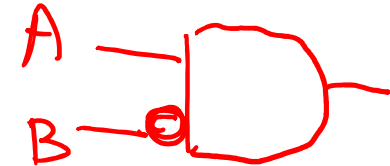
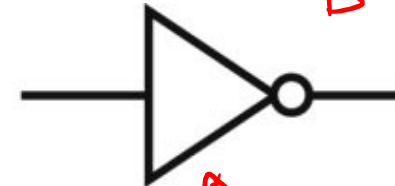
Do
NAND

OR



Do
NOR

NOT



Source: H&P textbook

What logic function is this?



OR



Source: H&P textbook

$$(\overline{A} + B)$$

Boolean Equation

- Consider the logic block that has an output E that is true only if exactly two of the three inputs A, B, C are true

Multiple correct equations:

Two must be true, but all three cannot be true:

$$E = ((A \cdot B) + (B \cdot C) + (A \cdot C)) \cdot \overline{(A \cdot B \cdot C)}$$

0 if $A=B=C=1$

Identify the three cases where it is true:

$$E = (A \cdot B \cdot \overline{C}) + (A \cdot C \cdot \overline{B}) + (C \cdot B \cdot \overline{A})$$

Sum of Products

product of
sums

where the cases
output = 0

$$(A+B+C) \cdot (A+B+\bar{C}) \cdot (A+\bar{B}+C) \cdot (\bar{A}+B+C) \cdot (\bar{A}+\bar{B}+\bar{C})$$

- Can represent any logic block with the AND, OR, NOT operators

- Draw the truth table
- For each true output, represent the corresponding inputs as a product
- The final equation is a sum of these products

describes the cases where output = 1 if

↓
A=0
B=1
C=1

A	B	C	E
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$$(A \cdot B \cdot \bar{C}) + (A \cdot C \cdot \bar{B}) + (C \cdot B \cdot \bar{A})$$

- Can also use "product of sums"
- Any equation can be implemented with an array of ANDs, followed by an array of ORs

NAND and NOR

- NAND : NOT of AND : $A \text{ nand } B = \overline{A \cdot B}$
- NOR : NOT of OR : $A \text{ nor } B = \overline{A + B}$
- NAND and NOR are *universal gates*, i.e., they can be used to construct any complex logical function

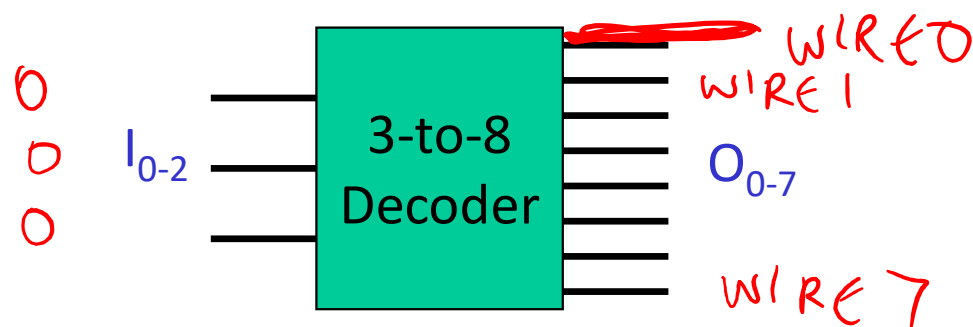
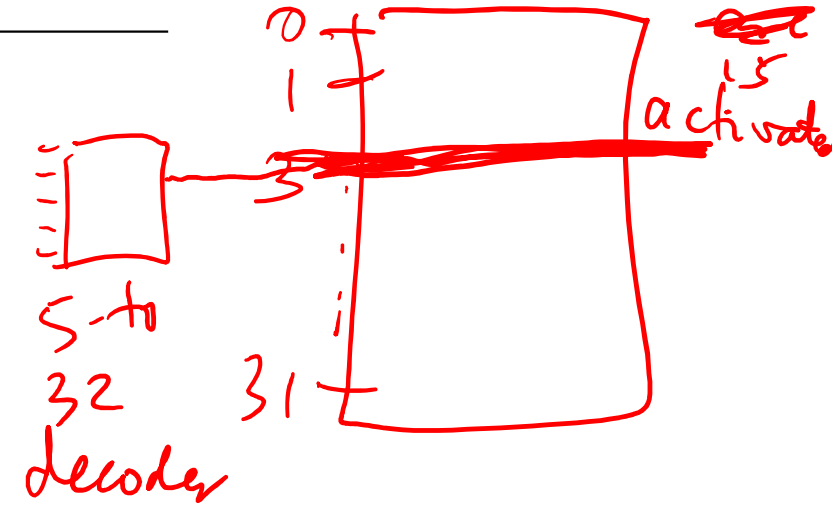
Common Logic Blocks – Decoder

Takes in N inputs and activates one of 2^N outputs

Storage ccts need a

decoder
input = addr
out = 1 of many addr

I_0	I_1	I_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



$$O_0 = I_0 \cdot I_1 \cdot I_2$$

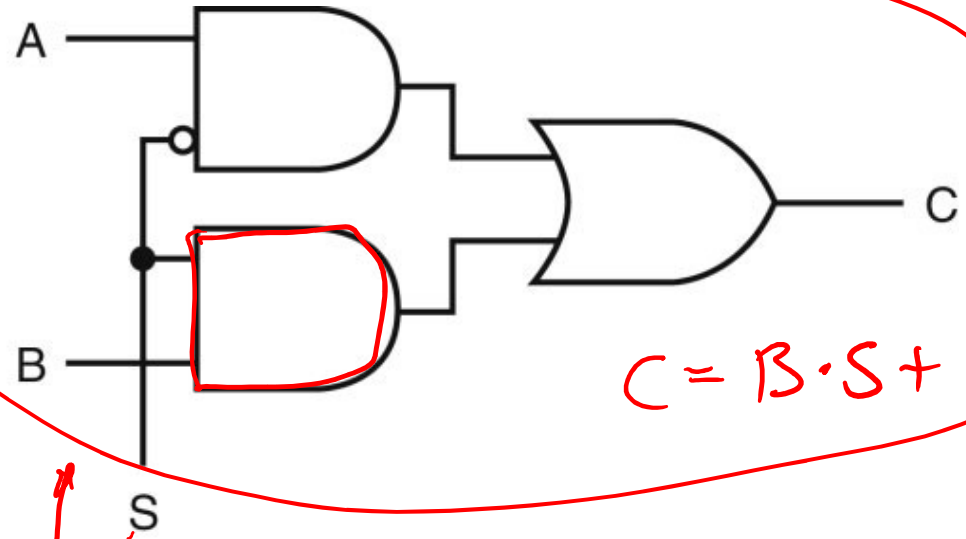
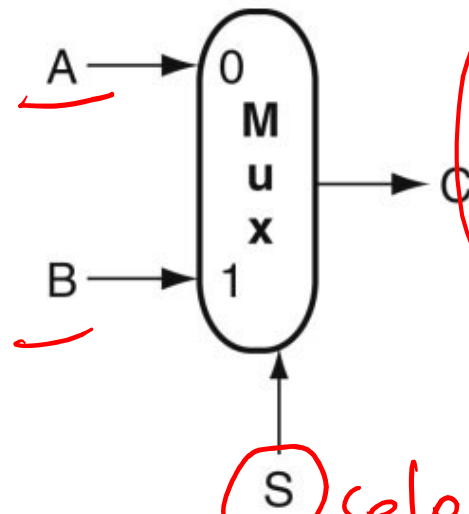
(sum of prod)

Common Logic Blocks – Multiplexor

A	B	S	C
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

- Multiplexor or selector: one of N inputs is reflected on the output depending on the value of the $\log_2 N$ selector bits

Design the
cct for
a
4 to 1
MUX



$$C = B \cdot S + A \cdot \bar{S}$$

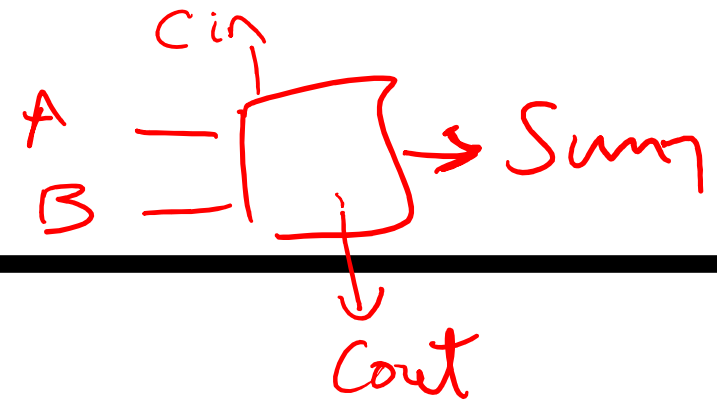
Source: H&P textbook

if (S == 00) then E = A
if (S == 01) then E = B
if (S == 10) E = C
if (S == 11) E = D

2-input mux

{ if S == 0, then C = A
if S == 1, then C = B

Adder Algorithm



	1	0	0	1
	0	1	0	1
Sum	1	1	1	0
Carry	0	0	0	1

Handwritten annotations: A red circle around the '0' in the third column of the Sum row. A red circle around the '0' in the third column of the Carry row. Arrows point from these circles to the '0' in the first column of the Carry row. A red '0' is written above the first column. A red squiggle is under the '1' in the fourth column of the Carry row.

Truth Table for the above operations:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Handwritten annotations: A red arrow points from the row (0, 1, 1) to the row (1, 0, 1). Red underlines are under the first and last rows of the table.

Handwritten text: 'Cout Sum' followed by a space and then '1 0'.

Adder Algorithm

$$\frac{A \cdot B \cdot C_{in} + A \cdot B \cdot \bar{C}_{in}}{= A \cdot B \cdot (C_{in} + \bar{C}_{in})}$$

$$= A \cdot B$$

$$A \cdot B \cdot C_{in} = A \cdot B \cdot C_{in} + A \cdot B \cdot \bar{C}_{in} + A \cdot B \cdot C_{in}$$

Equations:

$$\text{Sum} = C_{in} \cdot \bar{A} \cdot \bar{B} + B \cdot \bar{C}_{in} \cdot \bar{A} + A \cdot \bar{C}_{in} \cdot \bar{B} + A \cdot B \cdot C_{in}$$

$$\text{Cout} = A \cdot B \cdot C_{in} + A \cdot B \cdot \bar{C}_{in} + A \cdot C_{in} \cdot \bar{B} + B \cdot C_{in} \cdot \bar{A}$$

$$= A \cdot B + A \cdot C_{in} + B \cdot C_{in}$$

	1	0	0	1
	0	1	0	1
Sum	1	1	1	0
Carry	0	0	0	1

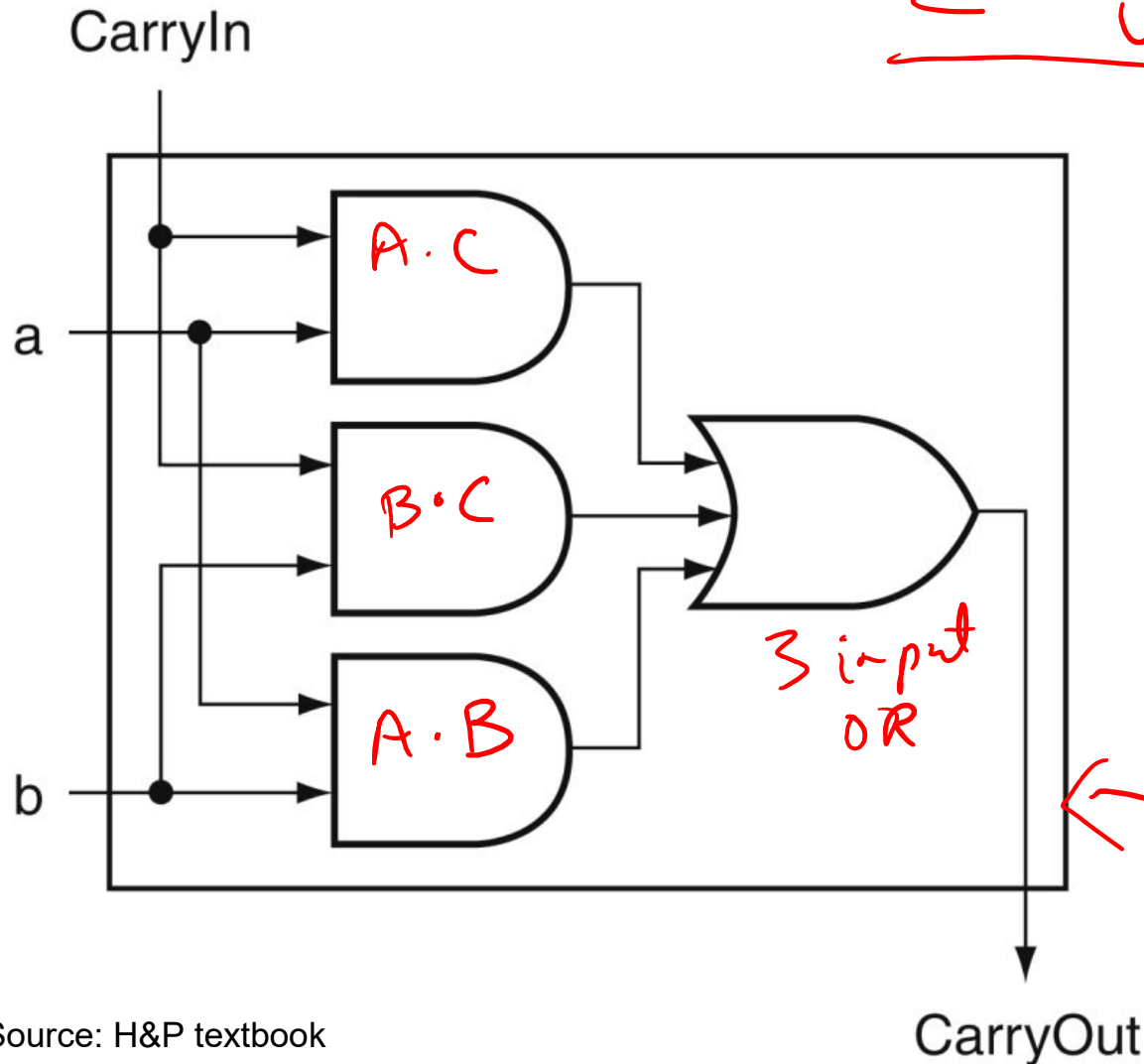
Truth Table for the above operations:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Carry Out Logic

Adding 2 input bits
(and carry-in)

= 2 gate delays



Equations:

$$\text{Sum} = \text{Cin} \cdot \bar{A} \cdot \bar{B} + \\ B \cdot \bar{\text{Cin}} \cdot \bar{A} + \\ A \cdot \bar{\text{Cin}} \cdot B + \\ A \cdot B \cdot \text{Cin}$$

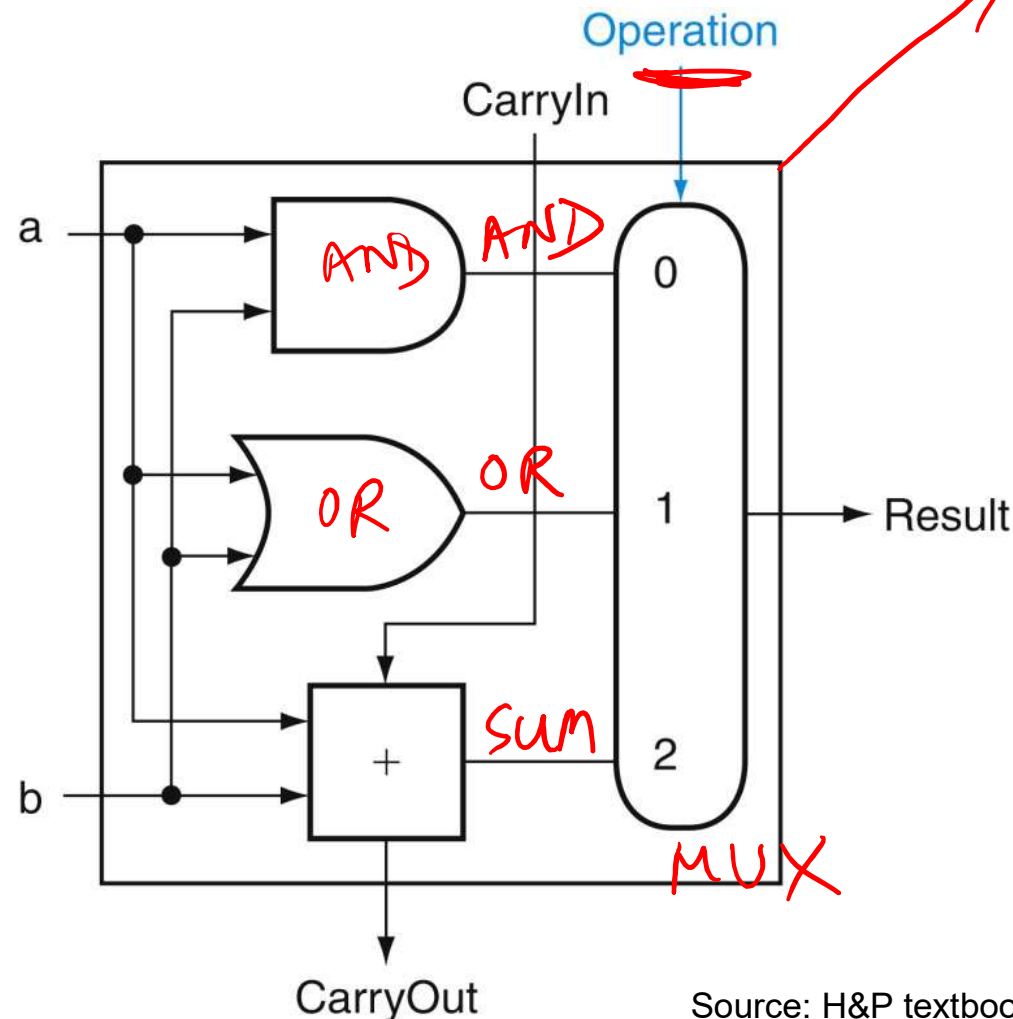
$$\text{Cout} = A \cdot B \cdot \text{Cin} + \\ A \cdot B \cdot \bar{\text{Cin}} + \\ A \cdot \text{Cin} \cdot \bar{B} + \\ B \cdot \text{Cin} \cdot \bar{A}$$

$$= \underline{A \cdot B} + \\ \underline{A \cdot \text{Cin}} + \\ \underline{B \cdot \text{Cin}}$$

Source: H&P textbook

1-Bit ALU with Add, Or, And

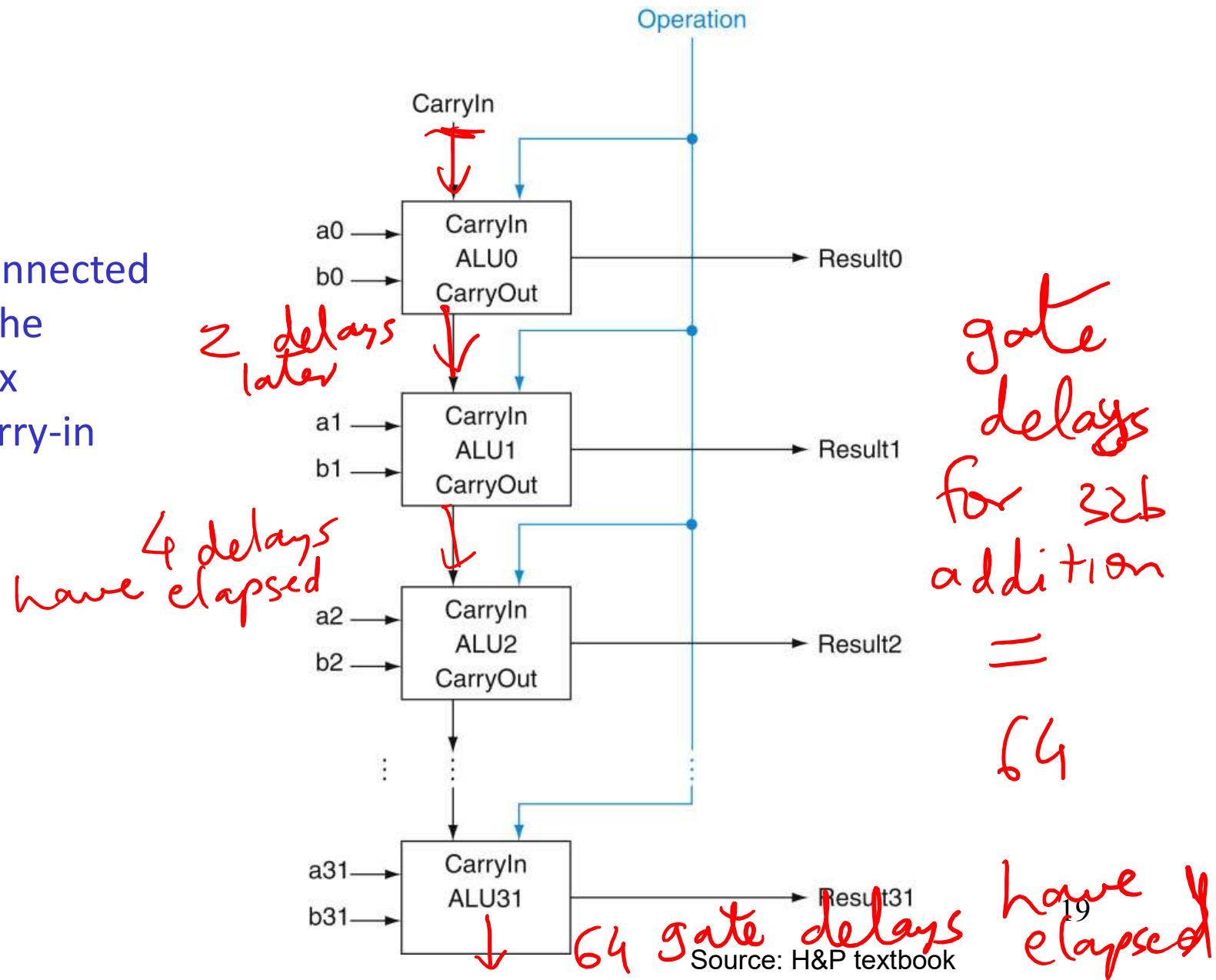
- Multiplexor selects between Add, Or, And operations



1 bit
Add
also
AND
OR

32-bit Ripple Carry Adder

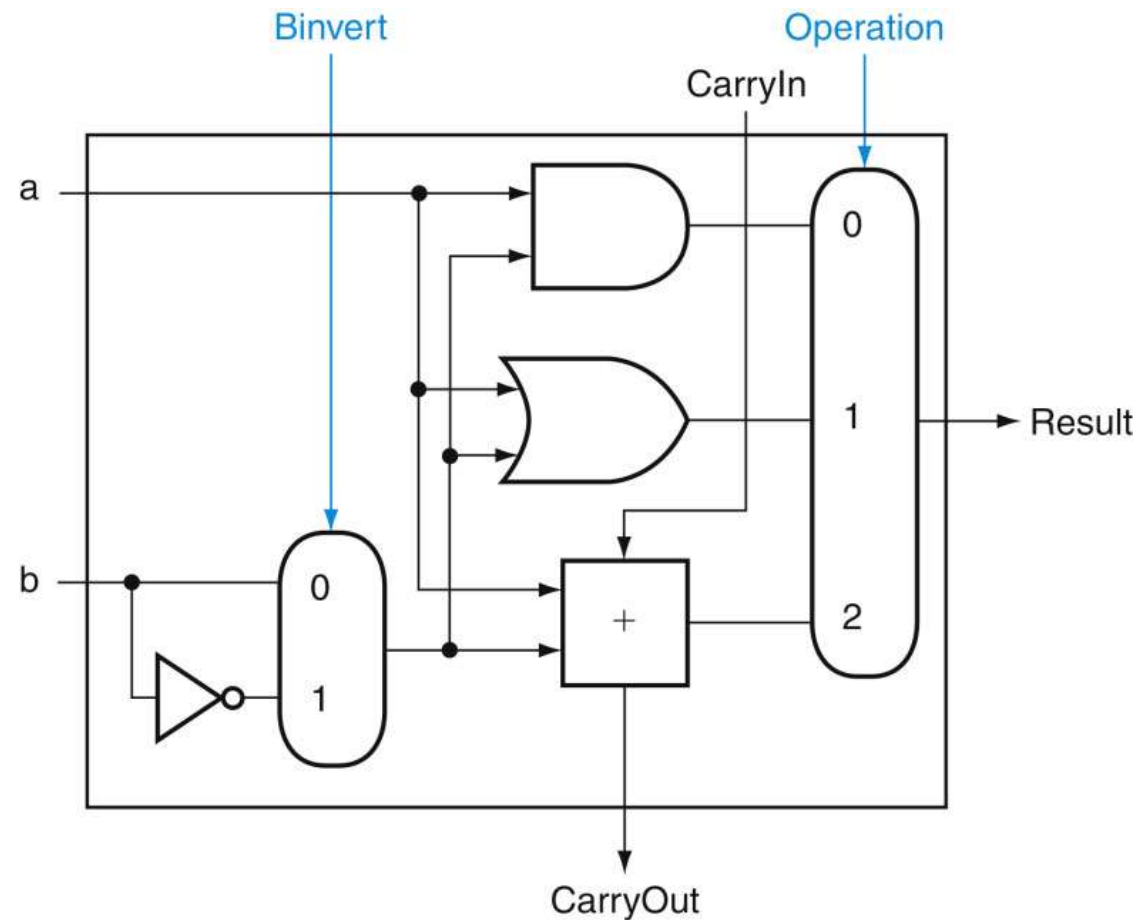
1-bit ALUs are connected
“in series” with the
carry-out of 1 box
going into the carry-in
of the next box



Incorporating Subtraction

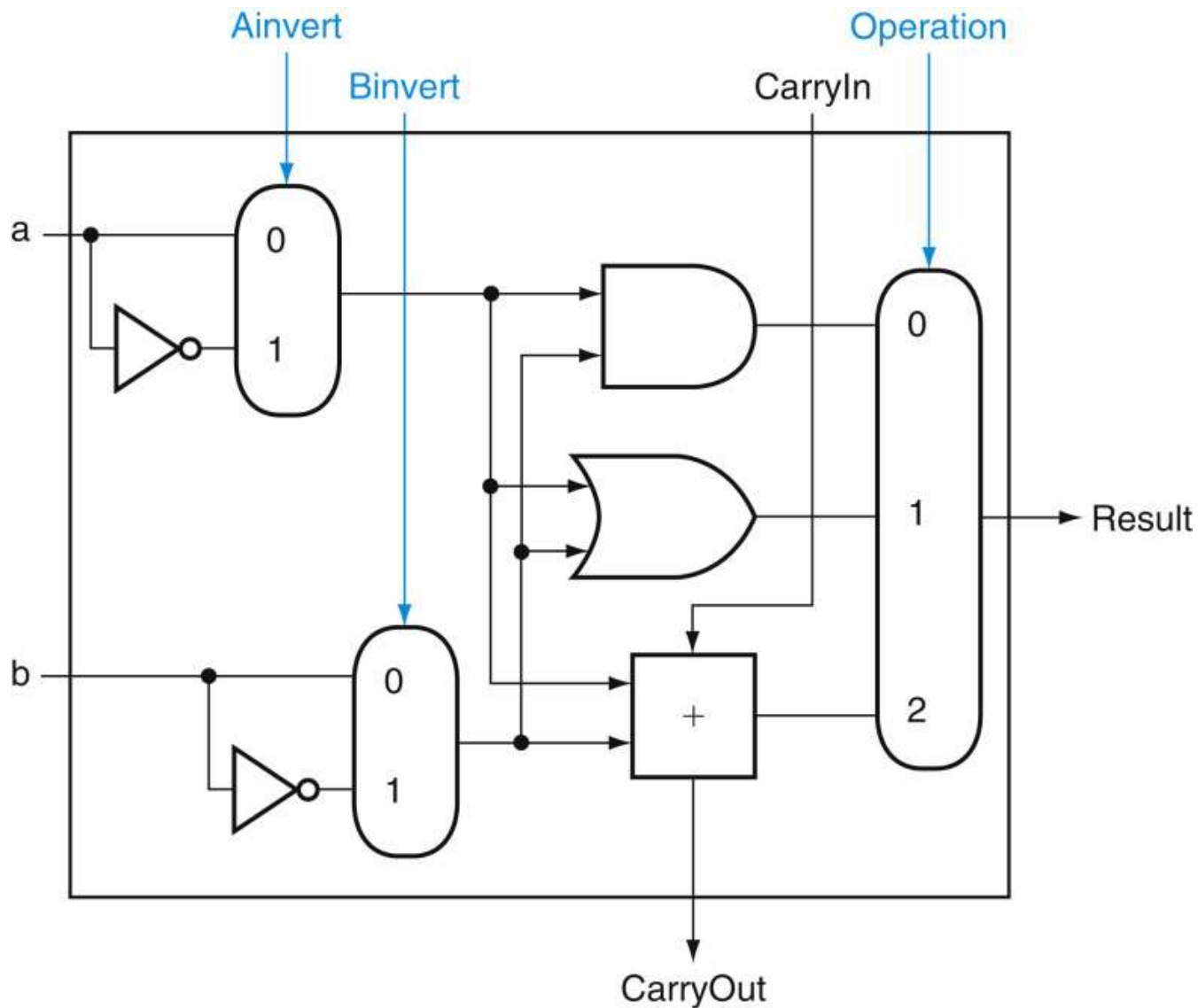
Must invert bits of B and add a 1

- Include an inverter
- CarryIn for the first bit is 1
- The CarryIn signal (for the first bit) can be the same as the Binvert signal



Source: H&P textbook

Incorporating NOR and NAND



Control Lines

What are the values of the control lines and what operations do they correspond to?

	Ai	Bn	Op
AND	0	0	00
OR	0	0	01
Add	0	0	10
Sub	0	1	10
NAND	1	1	01
NOR	1	1	00

