

Lecture 5: More Instructions, Procedure Calls

- Today's topics:

- Examples
- Numbers, control instructions
- Procedure calls

HW 2 posted (due next Tuesday)

HW 1 solns posted later today (Canvas)

Sign up on Piazza

0000 100 111
 2^5 2^4 2^3 2^2 2^1 2^0

~~39~~ ~~10011110~~ $39_{10} \rightarrow \text{binary}$

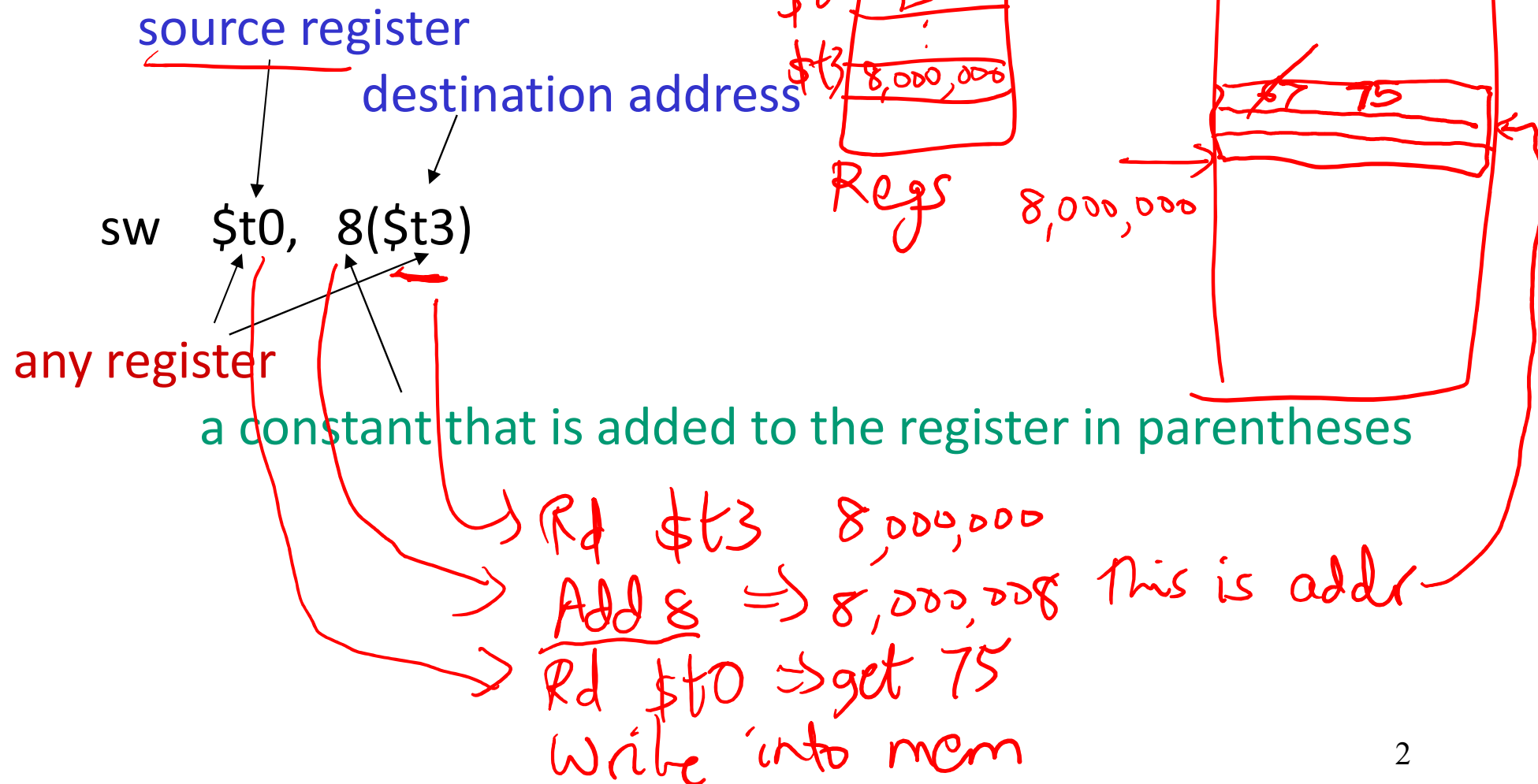
$$\begin{array}{rcl} 39 \div 2 & = & 19 \text{ rem } 1 \\ 19 \div 2 & = & 9 \text{ rem } 1 \\ 9 \div 2 & = & 4 \text{ rem } 1 \\ 4 \div 2 & = & 2 \text{ rem } 0 \\ 2 \div 2 & = & 1 \text{ rem } 0 \end{array}$$

last bit

$$\begin{array}{rcl} 1 \div 2 & = & 0 \text{ rem } 1 \\ 0 \div 2 & = & 0 \text{ rem } 0 \\ 0 \div 2 & = & 0 \text{ rem } 0 \end{array}$$

Memory Instruction Format

- The format of a store instruction:



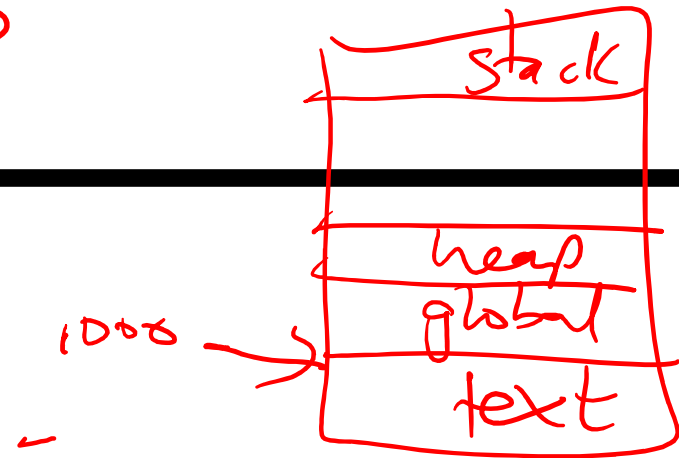
Example

each int is 4B

int a, b, c, d[10];

~~addi~~ ~~\$gp~~, \$zero, 1000 # assume that data is stored at
base address 1000; placed in \$gp;
\$zero is a register that always
equals zero

→ lw \$s1, 0(\$gp) # brings value of a into register \$s1
lw \$s2, 4(\$gp) # brings value of b into register \$s2
lw \$s3, 8(\$gp) # brings value of c into register \$s3
lw \$s4, 12(\$gp) # brings value of d[0] into register \$s4
lw \$s5, 16(\$gp) # brings value of d[1] into register \$s5



Example

int a, b, c, d[10] \rightarrow prod 6 lines of code

Convert to assembly:

C code: d[3] = d[2] + a;

lw

~~rx~~ $\leftarrow a$

lw

$\leftarrow d[2]$

add regs regs regs

sw

$\rightarrow d[3]$

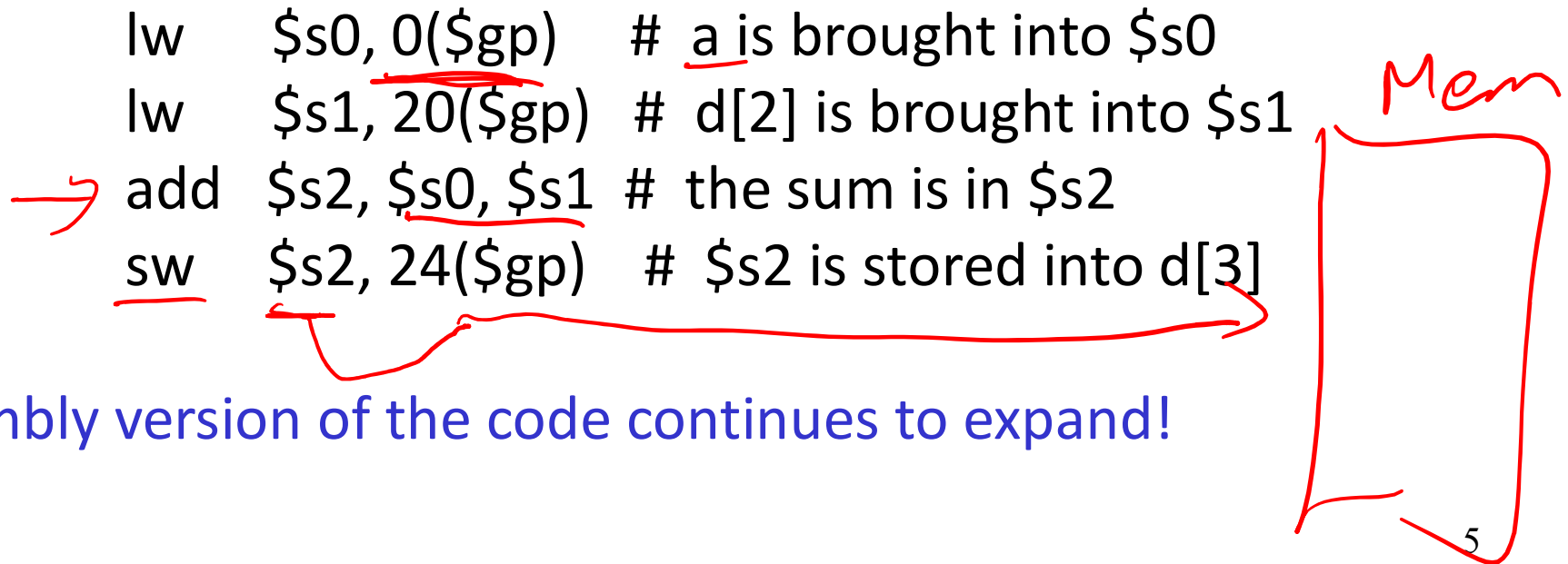
Example

Convert to assembly:

C code: `d[3] = d[2] + a;`

Assembly (same assumptions as previous example):

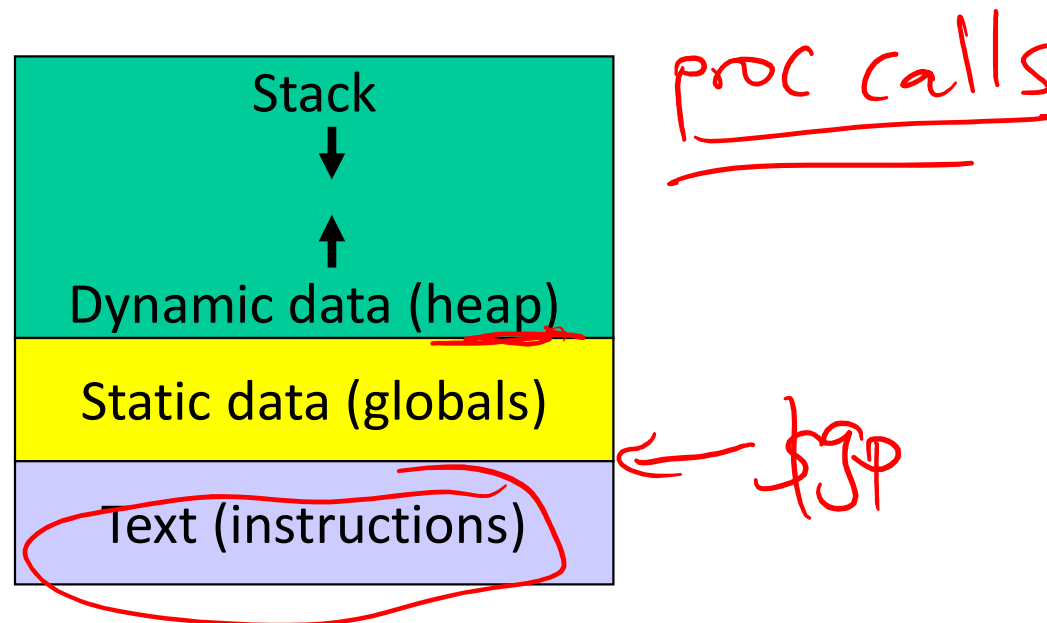
```
lw    $s0, 0($gp)    # a is brought into $s0
lw    $s1, 20($gp)   # d[2] is brought into $s1
→ add  $s2, $s0, $s1  # the sum is in $s2
sw   $s2, 24($gp)  # $s2 is stored into d[3]
```



Assembly version of the code continues to expand!

Memory Organization

- The space allocated on stack by a procedure is termed the activation record (includes saved values and data local to the procedure) – frame pointer points to the start of the record and stack pointer points to the end – variable addresses are specified relative to \$fp as \$sp may change during the execution of the procedure
- \$gp points to area in memory that saves global variables
- Dynamically allocated storage (with malloc()) is placed on the heap



Recap – Numeric Representations 0x 4b $4 \times 16^1 + b \times 16^0$

- Decimal ~~75~~ $35_{10} = 3 \times 10^1 + 5 \times 10^0$

$$75 = 64 + 11$$

$$= 4 \times 16 + 11 \times 1$$

$$\rightarrow 0x 2^2$$

- Binary $00100011_2 = 1 \times 2^5 + 1 \times 2^1 + 1 \times 2^0$

8-bit

- Hexadecimal (compact representation)

$$\underline{0x 23} \text{ or } \underline{23}_{\text{hex}} = 2 \times 16^1 + 3 \times 16^0$$

0-15 (decimal) \rightarrow 0-9, a-f (hex)

$$\begin{array}{|c|c|} \hline 0010 & 0011 \\ \hline 2 & 3 \end{array}$$

Dec	Binary	Hex	Dec	Binary	Hex	Dec	Binary	Hex	Dec	Binary	Hex
0	0000	00	4	0100	04	8	1000	<u>08</u>	12	1100	0c
1	0001	01	5	0101	05	9	1001	<u>09</u>	13	1101	0d
2	0010	02	6	0110	06	10	1010	<u>0a</u>	14	1110	0e
3	0011	03	7	0111	07	<u>11</u>	1011	<u>0b</u>	15	1111	0f

Instruction Formats

32 regs

00000
00001
.
.

31 → 1 1 1 1 1

Instructions are represented as 32-bit numbers (one word), broken into 6 fields

R-type instruction

add \$t0, \$s1, \$s2

000000 10001 10010 01000 00000 100000

6 bits 5 bits 5 bits 5 bits 5 bits 6 bits

op rs rt rd shamt funct

opcode source source dest shift amt function

I-type instruction

lw \$t0, 32(\$s3)

6 bits 5 bits 5 bits

opcode rs rt

(\$s3) (\$t0)

16 bits
constant

Instr are
regular &
simple

Logical Operations

Dec 17 sll by 3
17000 $\Rightarrow 17 \times 10^3$

8 17,416

srl 5 \rightarrow 8

Logical ops

C operators

Java operators

MIPS instr

Shift Left

<<

<<

Shift Right

>>

>>>

Bit-by-bit AND

&

&

Bit-by-bit OR

|

|

Bit-by-bit NOT

~

~

sll

srl

and, andi

or, ori

nor (with \$zero)

srl by 5
 \div by 2^5

sll \$s1, \$s2, 3

3
2 X

\$s2

0 00011

↓ shift left by 3

\$s1

0 00011000

Control Instructions

- Conditional branch: Jump to instruction L1 if register1 equals register2: beq register1, register2, L1
Similarly, bne and slt (set-on-less-than)

Pseudo instr bit

- Unconditional branch:

j L1

jr \$s0 (useful for big jumps and procedure returns)

Convert to assembly:

```
if (i == j)
    f = g+h;
else
    f = g-h;
```

slt
beq

16 bytes away
then

else

then2

else2

j 16
assembler

J then

Control Instructions

- Conditional branch: Jump to instruction L1 if register1 equals register2: `beq register1, register2, L1`
Similarly, `bne` and `slt` (set-on-less-than)
- Unconditional branch:
`j L1`
`jr $s0` (useful for big jumps and procedure returns)

Convert to assembly:

```
if (i == j)
    f = g+h;
else
    f = g-h;
```

```
→ bne $s3, $s4, Else
then: add $s0, $s1, $s2 ←
      j End
Else: sub $s0, $s1, $s2 ←
End:
```

Example

save[i]

Convert to assembly:

```
while (save[i] == k)
    i += 1;
```

Values of i and k are in \$s3
and \$s5 and base of array
save[] is in \$s6

\$s6 has addr of start of save[i]
addr of save[0]

addr of save[1] = $\$s6 + 4$
 $4(\$s6)$

addr of save[2] = $8(\$s6)$
 $\$s6 + 8$

addr of save[i] = $\$s6 + 4i$

Example

$sll\ by\ 2 \Rightarrow mult\ by\ 2^2$

Convert to assembly:

while (save[i] == k)
i += 1;

Values of i and k are in \$s3
and \$s5 and base of array
save[] is in \$s6

```
Loop: sll    $t1, $s3, 2  
      add    $t1, $t1, $s6  
      lw     $t0, 0($t1)  
      bne    $t0, $s5, Exit  
      addi   $s3, $s3, 1  
      j      Loop
```

Exit:

```
      sll    $t1, $s3, 2  
      add    $t1, $t1, $s6  
Loop: lw     $t0, 0($t1)  
      bne    $t0, $s5, Exit  
      addi   $s3, $s3, 1  
      addi   $t1, $t1, 4  
      j      Loop
```

Exit:

\$s6
+ 4i

calc
4i

incr
i

addr the
addr of
save[i]

13

\$t1
pointing to
addr of save[i]

lw
save[i] simpler
addr of save[i]
= \$s6 + 4i
\$t1

Registers

- The 32 MIPS registers are partitioned as follows:
 - Register 0 : \$zero always stores the constant 0
 - Regs 2-3 : \$v0, \$v1 return values of a procedure
 - Regs 4-7 : \$a0-\$a3 input arguments to a procedure
 - Regs 8-15 : \$t0-\$t7 temporaries
 - Regs 16-23: \$s0-\$s7 variables
 - Regs 24-25: \$t8-\$t9 more temporaries
 - Reg 28 : \$gp global pointer
 - Reg 29 : \$sp stack pointer
 - Reg 30 : \$fp frame pointer
 - Reg 31 : \$ra return address

Procedures

- Local variables, AR, \$fp, \$sp
- Scratchpad and saves/restores
- Arguments and returns
- jal and \$ra