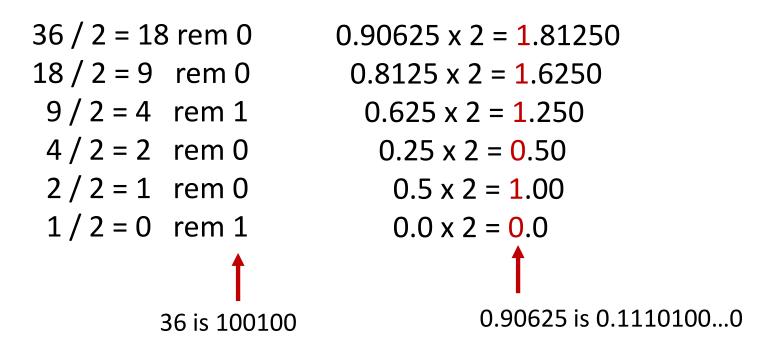
Lecture 11: Floating Point, Digital Design

1000 754 skipline • Today's topics: FP formats, arithmetic Intro to Boolean functions fra-pc+4 Sol 1 . data procA: wood 75 about \$9P la \$\$1, contevar

6x10 23 ÷ 2 = 11 rem + 4 x 10 750.9 11 -J-010 1 -7.509 x1025-22 0 7 -= 23) 2 = 2 1011 -4 rem O 1 - 7 0.647 -4 -> 123 $0 \div 7$ 0.647 × 2 = 1.294 6 $0.294 \times 2 = 0.588$ 0.588 × 2 = 1.176 642 11.10100.... 0.176 × 2 = 0.352 = KD 0352 × 2= 0.704 1.011110100 · ·· 1000 0011 0 1(110100 X Z 4

Final representation: (-1)^S x (1 + Fraction) x 2^(Exponent – Bias)

• Represent 36.90625_{ten} in single-precision format

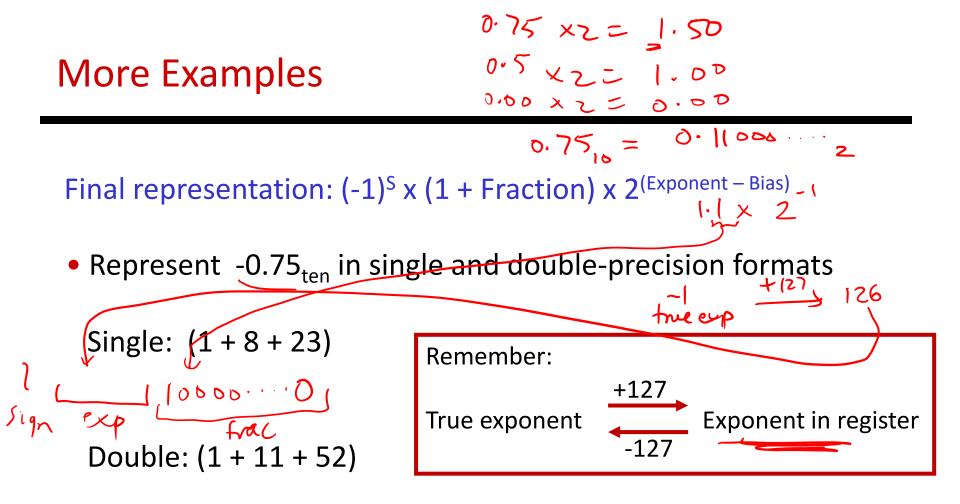


Final representation: (-1)^S x (1 + Fraction) x 2^(Exponent – Bias)

We've calculated that $36.90625_{ten} = 100100.1110100...0$ in binary Normalized form = $1.001001110100...0 \times 2^5$ (had to shift 5 places to get only one bit left of the point)

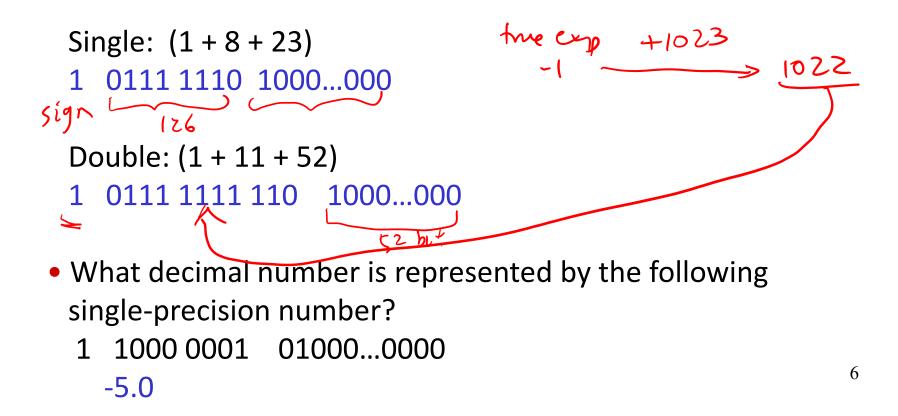
The sign bit is 0 (positive number) The fraction field is 001001110100...0 (the 23 bits after the point) The exponent field is 5 + 127 (have to add the bias) = 132, which in binary is 10000100 The IEEE 754 format is 0 10000100 001001110100.....0

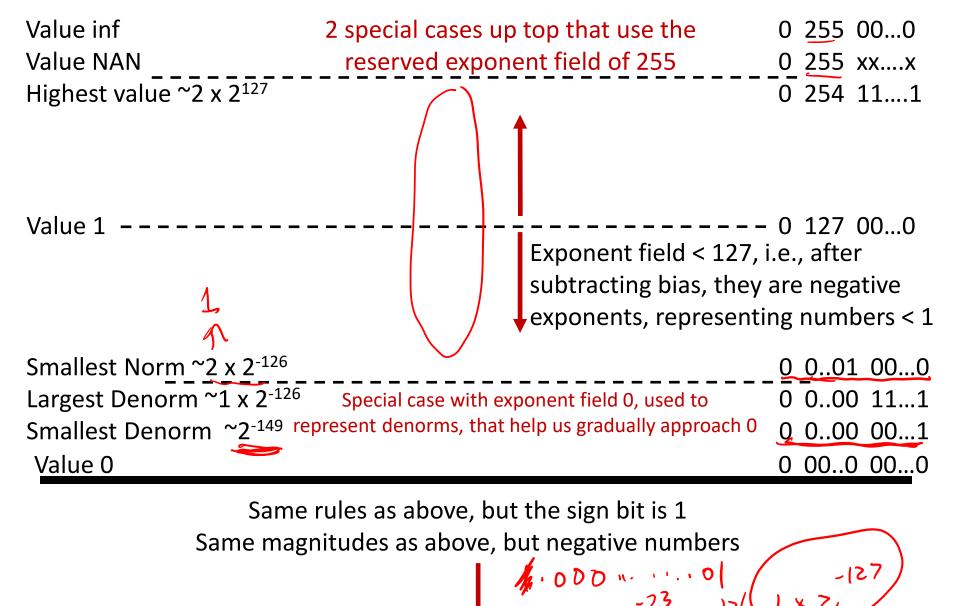
sign exponent 23 fraction bits



• What decimal number is represented by the following single-precision number? 1 1000 0001 01000...0000 = -101.00= -5 Final representation: (-1)^S x (1 + Fraction) x 2^(Exponent – Bias)

• Represent -0.75_{ten} in single and double-precision formats





FP Addition

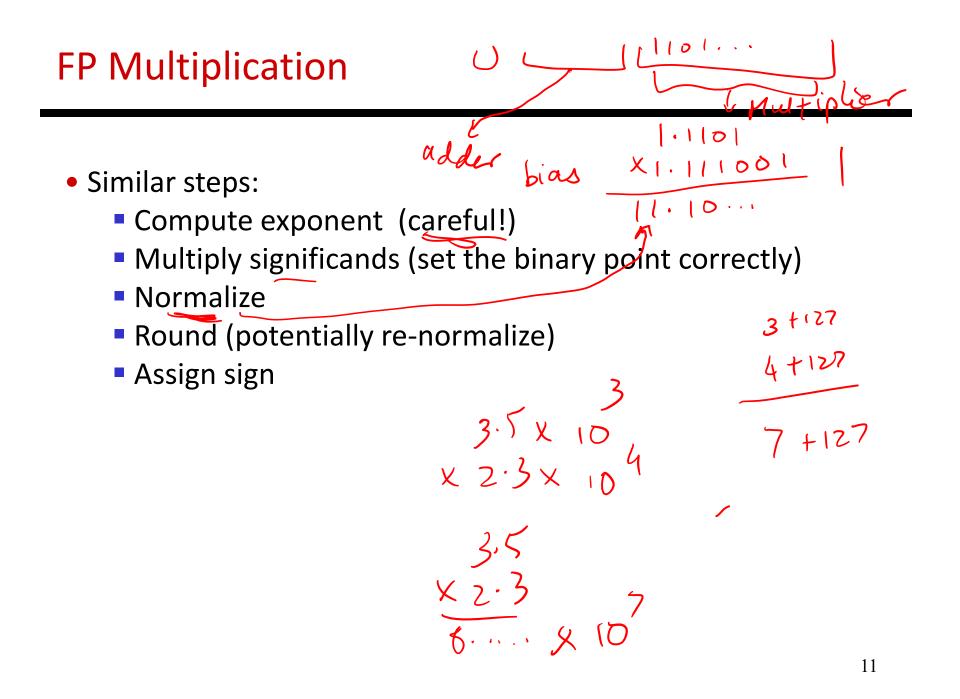
 Consider the following decimal example (can maintain only 4 decimal digits and 2 exponent digits) - exp left by 2 dú 9.999 x 10¹ 1.610 x 10⁻¹ +9.999 +2 Convert to the larger exponent: + 0.016 9.999 x 10^1 + 0.016 x 10^3 10.015 Add 10.015 x 10¹ Normalize 1.0015×10^2 Check for overflow/underflow Round 1.002×10^2 **Re-normalize**

 Consider the following decimal example (can maintain only 4 decimal digits and 2 exponent digits)

```
9.999 x 10^1 + 1.610 x 10^{-1}
Convert to the larger exponent:
9.999 x 10^1 + 0.016 x 10^1
Add
10.015 x 10<sup>1</sup>
                                       If we had more fraction bits,
Normalize
                                     these errors would be minimized
1.0015 \times 10^2
Check for overflow/underflow
Round
1.002 \times 10^2
Re-normalize
```

Consider the following binary example

```
1.010 \times 2^{1} + 1.100 \times 2^{3}
Convert to the larger exponent:
0.0101 \times 2^3 + 1.1000 \times 2^3
Add
1.1101 x 2<sup>3</sup>
Normalize
1.1101 x 2<sup>3</sup>
Check for overflow/underflow
Round
Re-normalize
```



MIPS Instructions

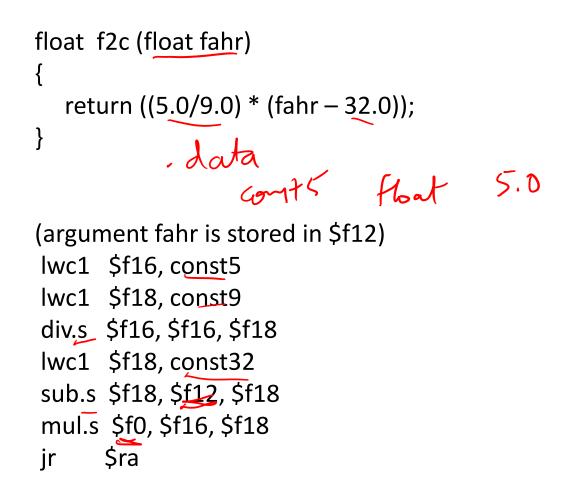
- The usual add.s, add.d, sub, mul, div
- Comparison instructions: c.eq.s, c.neq.s, c.lt.s.... These comparisons set an internal bit in hardware that is then inspected by branch instructions: bc1t, bc1f

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INT

- Separate register file \$f0 \$f31 : a double-precision value is stored in (say) \$f4-\$f5 and is referred to by \$f4
- Load/store instructions (lwc1, swc1) must still use integer registers for address computation





• FP operations are much slower than integer ops

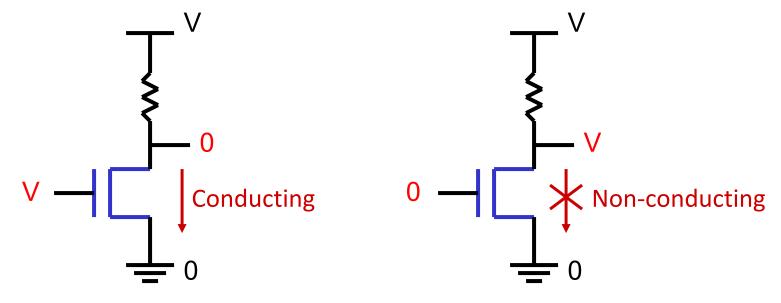
- Fixed point arithmetic uses integers, but assumes that every number is multiplied by the same factor
- Example: with a factor of 1/1000, the fixed-point representations for 1.46, 1.7198, and 5624 are respectively 1460, 1720, and 5624000
- More programming effort and possibly lower precision for higher performance

0,00337..

Subword Parallelism

- ALUs are typically designed to perform 64-bit or 128-bit arithmetic
 Some data types are much smaller, e.g., bytes for pixel
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 RGB values, half-words for audio samples
- Partitioning the carry-chains within the ALU can convert the 64-bit adder into 4 16-bit adders or 8 8-bit adders
- A single load can fetch multiple values, and a single add instruction can perform multiple parallel additions, referred to as subword parallelism

- Two voltage levels high and low (1 and 0, true and false) Hence, the use of binary arithmetic/logic in all computers
- A transistor is a 3-terminal device that acts as a switch



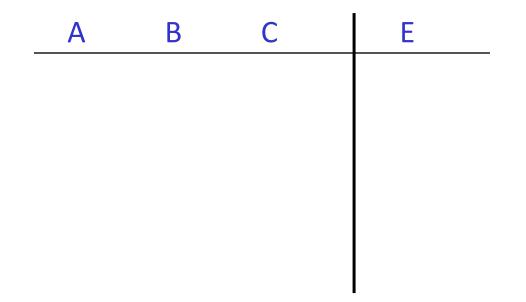


- A logic block has a number of binary inputs and produces a number of binary outputs – the simplest logic block is composed of a few transistors
- A logic block is termed *combinational* if the output is only a function of the inputs
- A logic block is termed *sequential* if the block has some internal memory (state) that also influences the output
- A basic logic block is termed a *gate* (AND, OR, NOT, etc.)

We will only deal with combinational circuits today



- A truth table defines the outputs of a logic block for each set of inputs
- Consider a block with 3 inputs A, B, C and an output E that is true only if *exactly* 2 inputs are true



Truth Table

- A truth table defines the outputs of a logic block for each set of inputs
- Consider a block with 3 inputs A, B, C and an output E that is true only if *exactly* 2 inputs are true

Α	В	С	E	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	Can be compressed by only
1	0	1	1	representing cases that
1	1	0	1	have an output of 1
1	1	1	0	
			1	19

- Equations involving two values and three primary operators:
 - OR : symbol + , X = A + B → X is true if at least one of A or B is true
 - AND : symbol . , X = A . B → X is true if both A and B are true

• NOT : symbol $\overline{}$, X = $\overline{A} \rightarrow X$ is the inverted value of A

Boolean Algebra Rules

- Identity law : A + 0 = A ; A . 1 = A
- Zero and One laws : A + 1 = 1 ; A . 0 = 0
- Inverse laws : $A \cdot \overline{A} = 0$; $A + \overline{A} = 1$
- Commutative laws : A + B = B + A ; A . B = B . A
- Associative laws : A + (B + C) = (A + B) + C
 A . (B . C) = (A . B) . C
- Distributive laws : A . (B + C) = (A . B) + (A . C)
 A + (B . C) = (A + B) . (A + C)

DeMorgan's Laws

• $\overline{A + B} = \overline{A} \cdot \overline{B}$

• $A \cdot B = A + B$

• Confirm that these are indeed true