

Lecture 11: Hardware for Arithmetic

- Today's topics:
 - Logic for common operations
 - Designing an ALU

Pictorial Representations

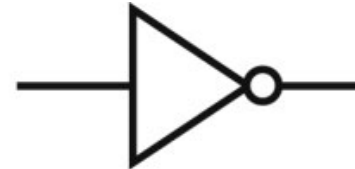
AND



OR



NOT



Source: H&P textbook

What logic function is this?



Source: H&P textbook

Boolean Equation

- Consider the logic block that has an output E that is true only if exactly two of the three inputs A, B, C are true

Multiple correct equations:

Two must be true, but all three cannot be true:

$$E = ((A \cdot B) + (B \cdot C) + (A \cdot C)) \cdot \overline{(A \cdot B \cdot C)}$$

Identify the three cases where it is true:

$$E = (A \cdot B \cdot \overline{C}) + (A \cdot C \cdot \overline{B}) + (C \cdot B \cdot \overline{A})$$

Sum of Products

- Can represent any logic block with the AND, OR, NOT operators
 - Draw the truth table
 - For each true output, represent the corresponding inputs as a product
 - The final equation is a sum of these products

A	B	C	E
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$$(A \cdot B \cdot \overline{C}) + (A \cdot C \cdot \overline{B}) + (C \cdot B \cdot \overline{A})$$

- Can also use “product of sums”
- Any equation can be implemented with an array of ANDs, followed by an array of ORs

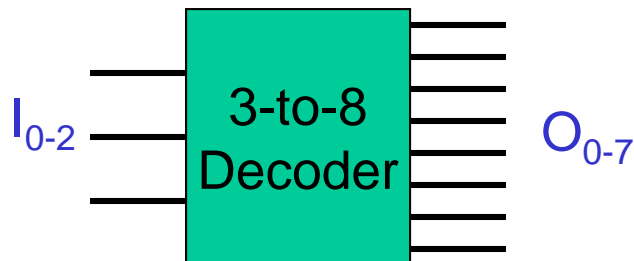
NAND and NOR

- NAND : NOT of AND : $A \text{ nand } B = \overline{A \cdot B}$
- NOR : NOT of OR : $A \text{ nor } B = \overline{A + B}$
- NAND and NOR are *universal gates*, i.e., they can be used to construct any complex logical function

Common Logic Blocks – Decoder

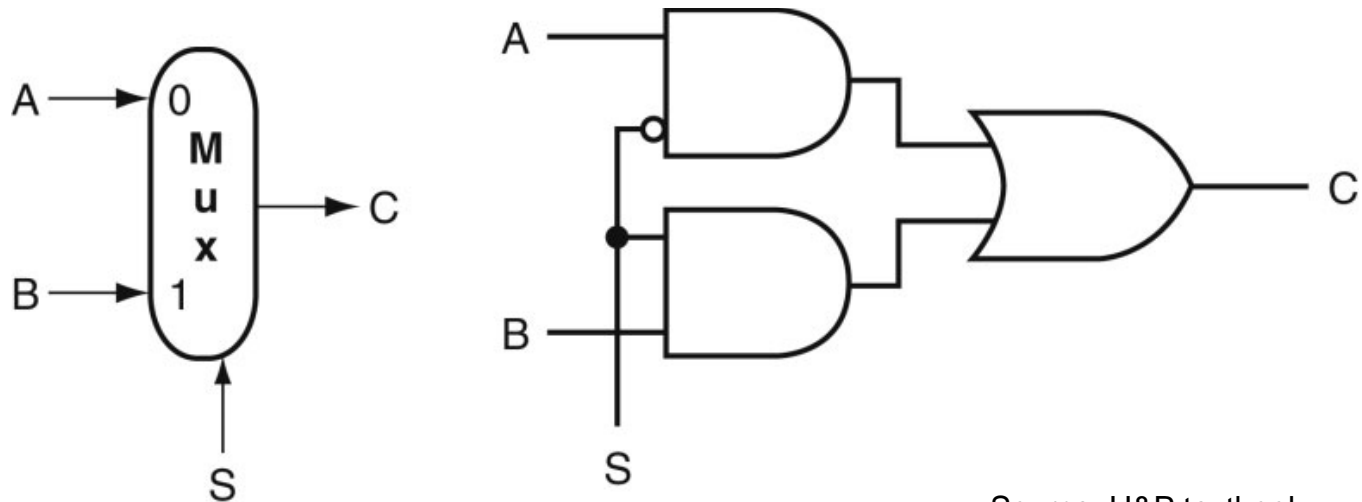
Takes in N inputs and activates one of 2^N outputs

I_0	I_1	I_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



Common Logic Blocks – Multiplexor

- Multiplexor or selector: one of N inputs is reflected on the output depending on the value of the $\log_2 N$ selector bits

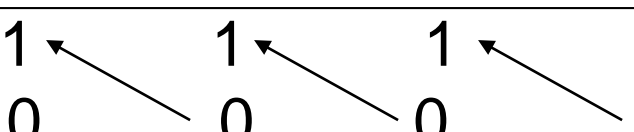


Source: H&P textbook

2-input mux

Adder Algorithm

	1	0	0	1
	0	1	0	1
Sum	1	1	1	0
Carry	0	0	0	1



Truth Table for the above operations:

A	B	Cin	Sum	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Adder Algorithm

	1	0	0	1
	0	1	0	1
Sum	1	1	1	0
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Truth Table for the above operations:

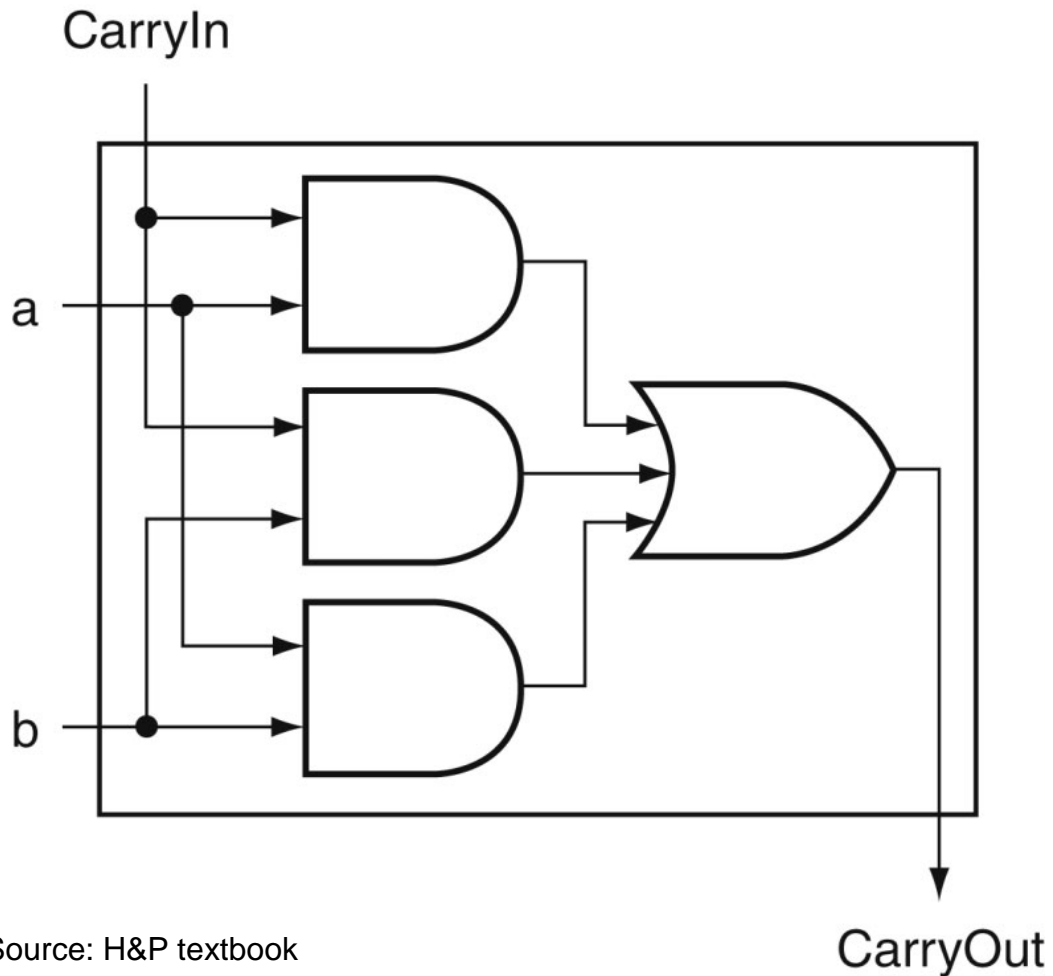
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equations:

$$\begin{aligned} \text{Sum} = & \text{Cin} \cdot \bar{A} \cdot \bar{B} + \\ & B \cdot \bar{\text{Cin}} \cdot \bar{A} + \\ & A \cdot \bar{\text{Cin}} \cdot \bar{B} + \\ & A \cdot B \cdot \text{Cin} \end{aligned}$$

$$\begin{aligned} \text{Cout} = & A \cdot B \cdot \text{Cin} + \\ & A \cdot B \cdot \bar{\text{Cin}} + \\ & A \cdot \text{Cin} \cdot \bar{B} + \\ & B \cdot \text{Cin} \cdot \bar{A} \\ = & A \cdot B + \\ & A \cdot \text{Cin} + \\ & B \cdot \text{Cin} \end{aligned}$$

Carry Out Logic



Equations:

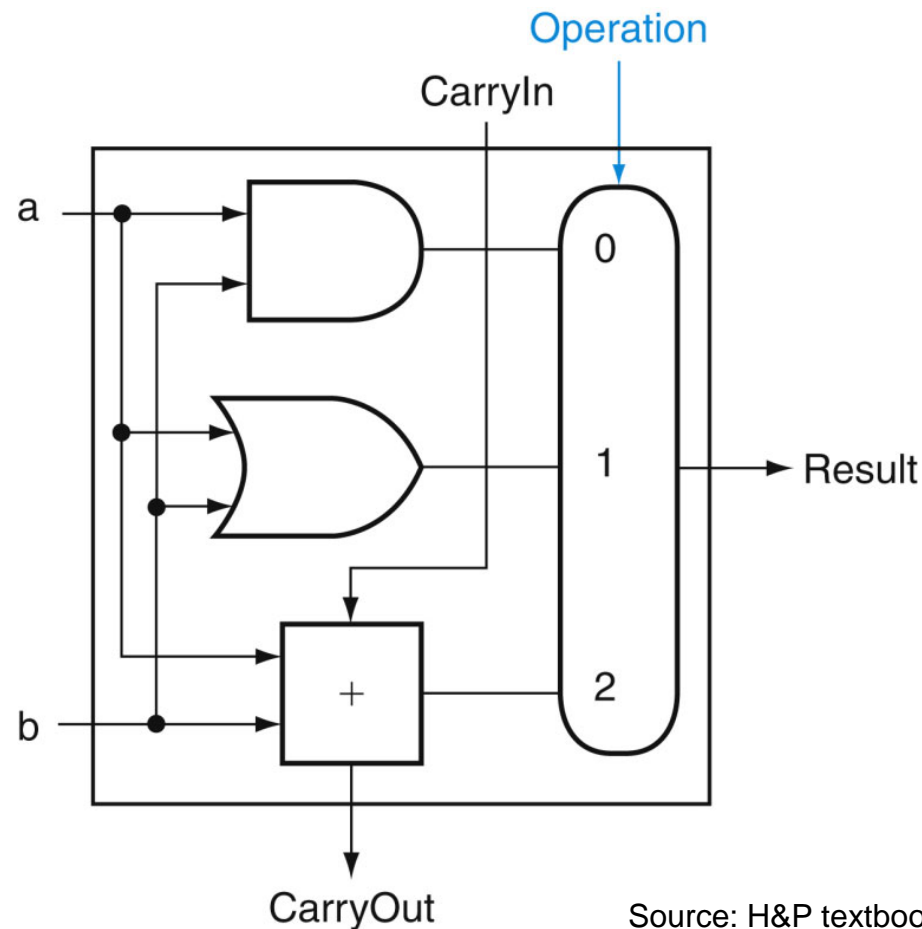
$$\begin{aligned} \text{Sum} = & \text{Cin} \cdot \bar{A} \cdot \bar{B} + \\ & B \cdot \bar{\text{Cin}} \cdot \bar{A} + \\ & A \cdot \bar{\text{Cin}} \cdot \bar{B} + \\ & A \cdot B \cdot \text{Cin} \end{aligned}$$

$$\begin{aligned} \text{Cout} = & A \cdot B \cdot \text{Cin} + \\ & A \cdot B \cdot \bar{\text{Cin}} + \\ & A \cdot \text{Cin} \cdot \bar{B} + \\ & B \cdot \text{Cin} \cdot \bar{A} \\ = & A \cdot B + \\ & A \cdot \text{Cin} + \\ & B \cdot \text{Cin} \end{aligned}$$

Source: H&P textbook

1-Bit ALU with Add, Or, And

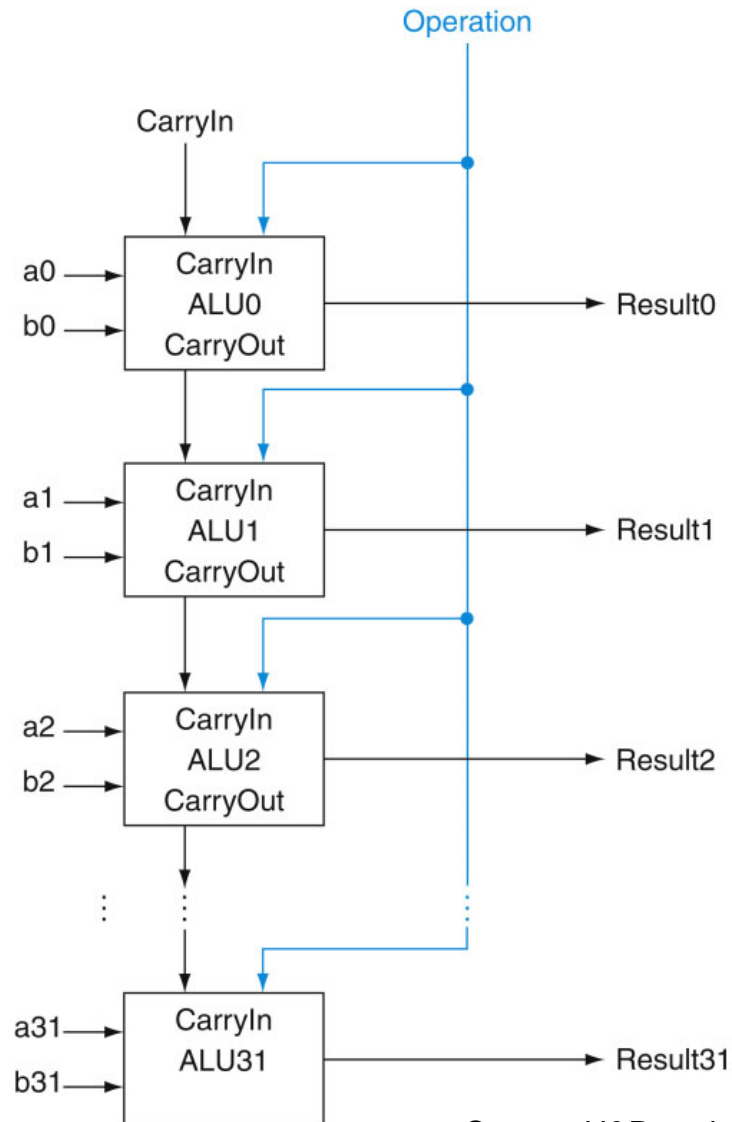
- Multiplexor selects between Add, Or, And operations



Source: H&P textbook

32-bit Ripple Carry Adder

1-bit ALUs are connected
“in series” with the
carry-out of 1 box
going into the carry-in
of the next box

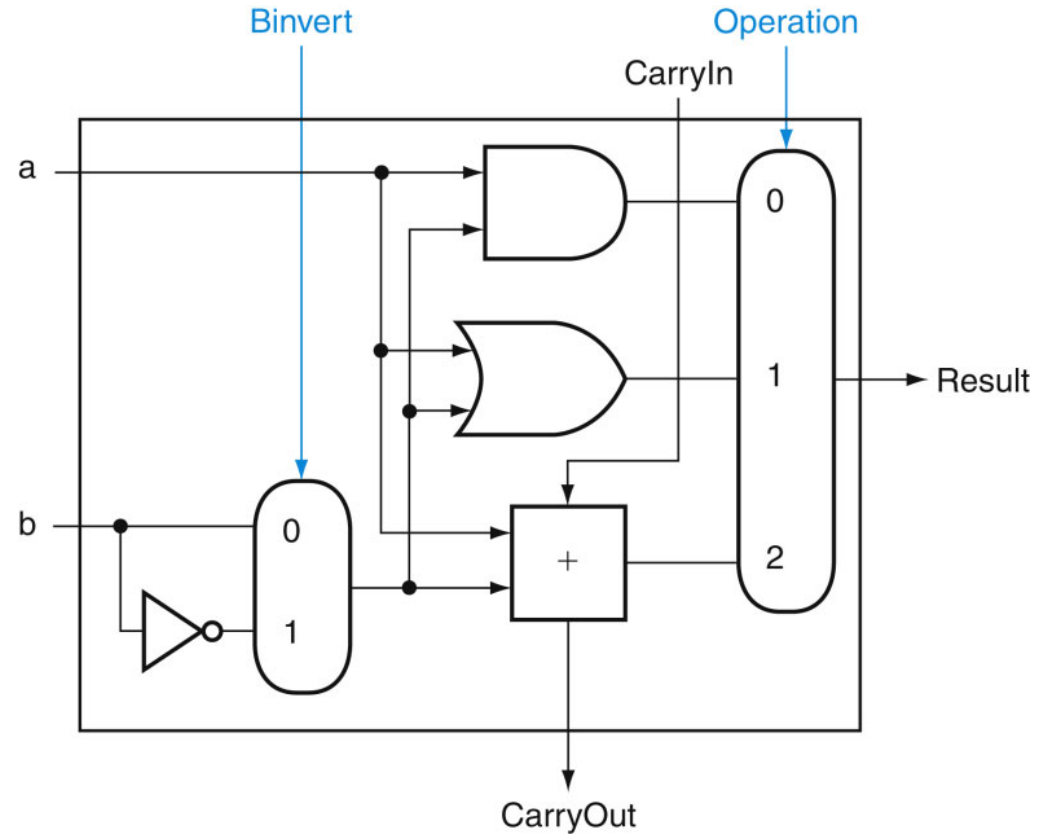


Source: H&P textbook

Incorporating Subtraction

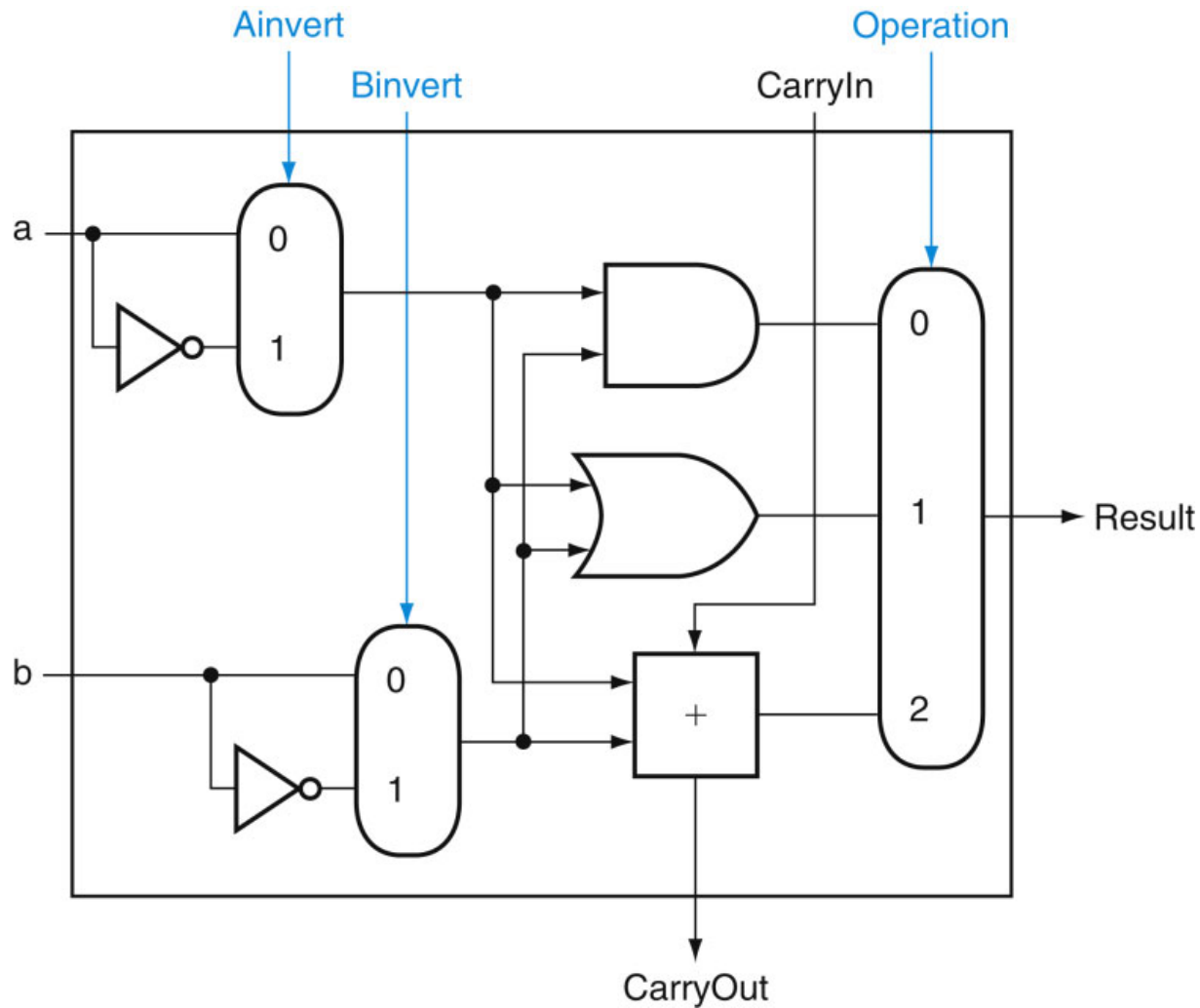
Must invert bits of B and add a 1

- Include an inverter
- CarryIn for the first bit is 1
- The CarryIn signal (for the first bit) can be the same as the Binvert signal



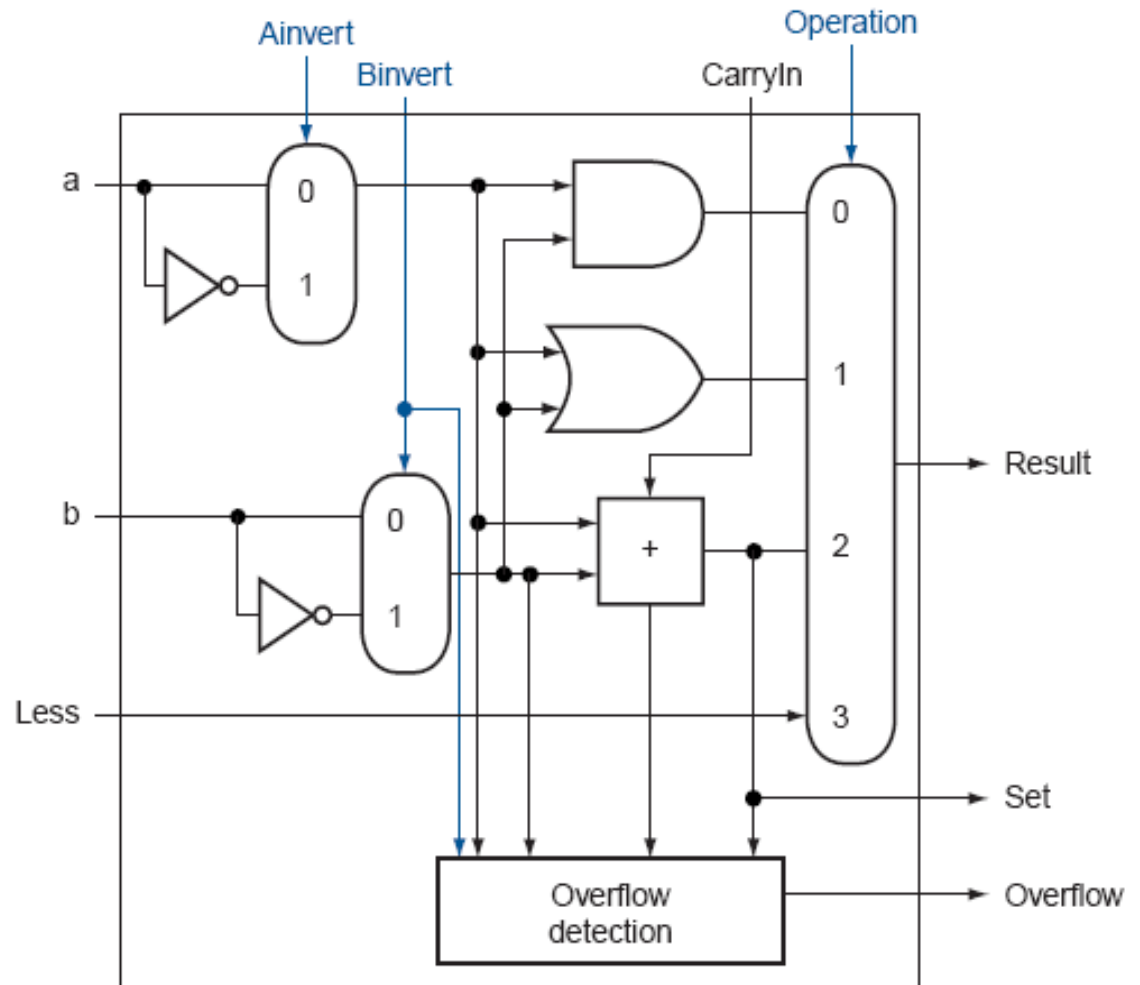
Source: H&P textbook

Incorporating NOR and NAND



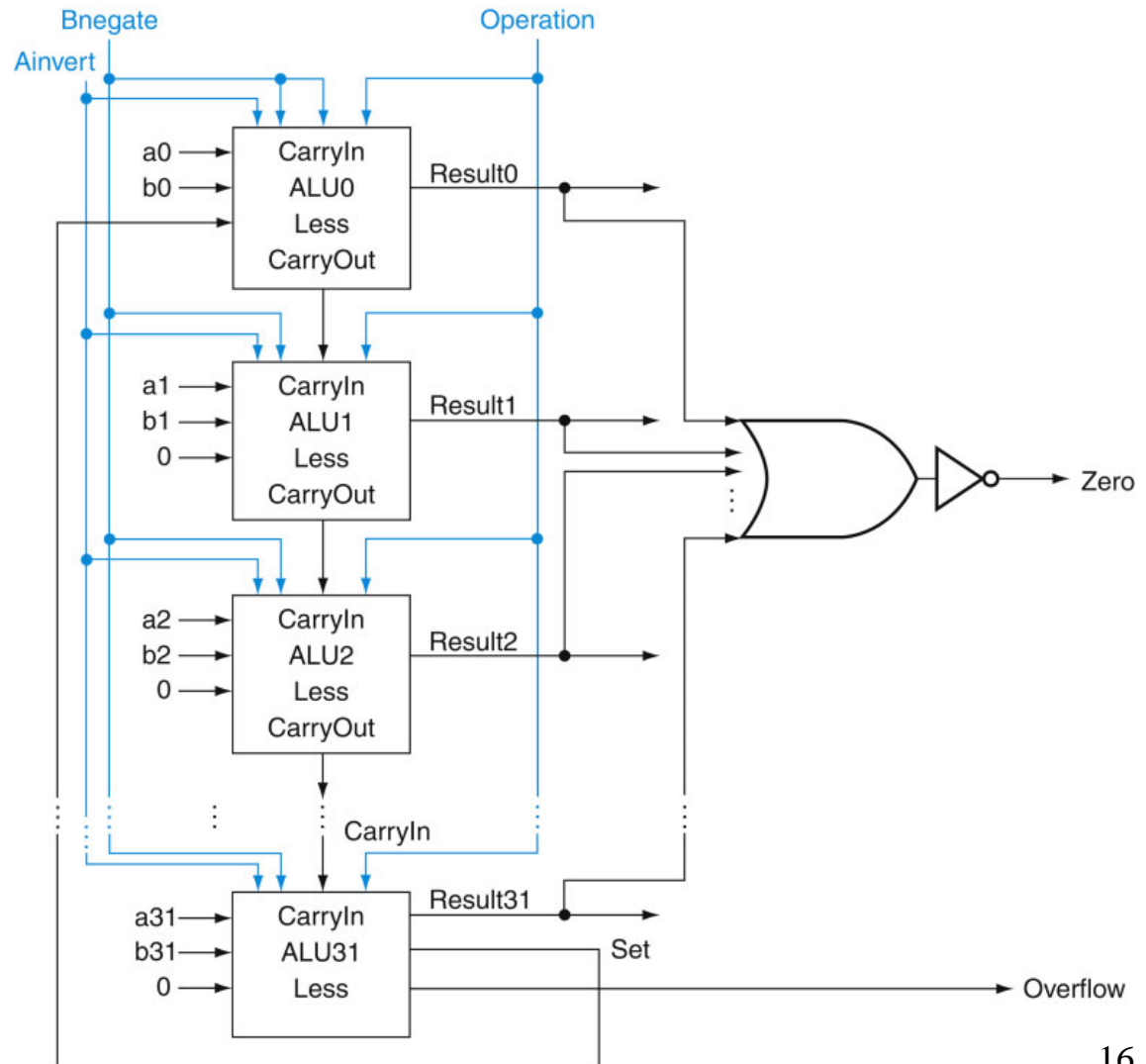
Incorporating slt

- Perform $a - b$ and check the sign
- New signal (Less) that is zero for ALU boxes 1-31
- The 31st box has a unit to detect overflow and sign – the sign bit serves as the Less signal for the 0th box



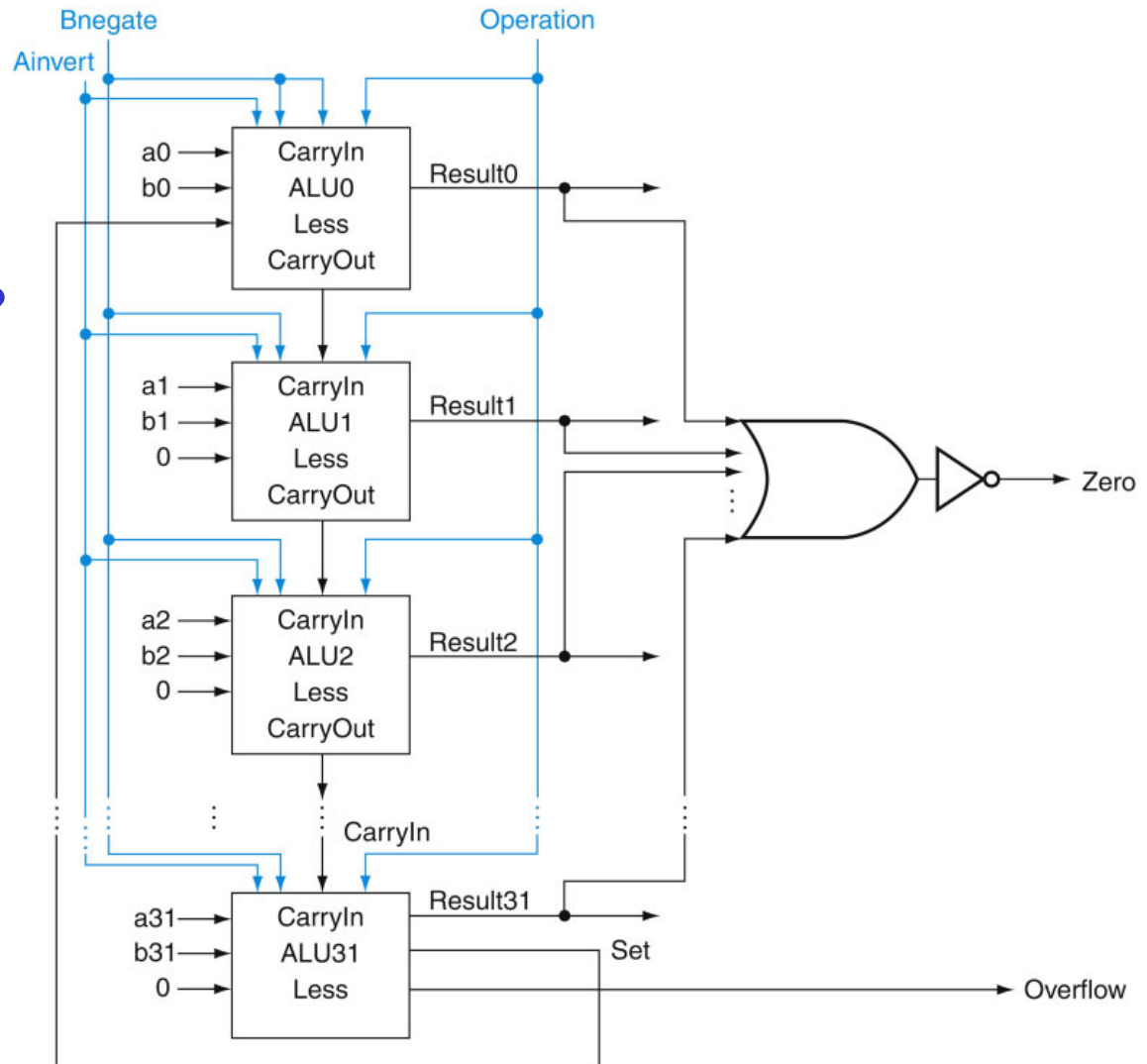
Incorporating beq

- Perform $a - b$ and confirm that the result is all zero's



Control Lines

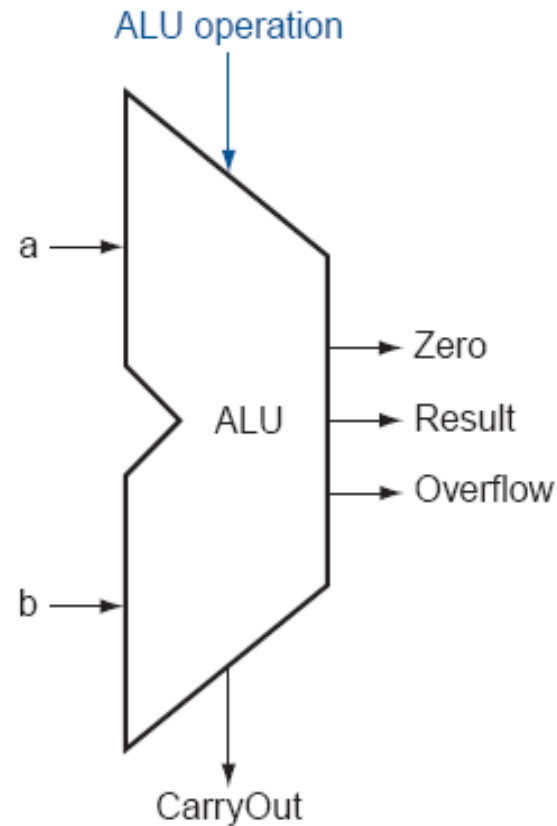
What are the values of the control lines and what operations do they correspond to?



Control Lines

What are the values of the control lines and what operations do they correspond to?

	Ai	Bn	Op
AND	0	0	00
OR	0	0	01
Add	0	0	10
Sub	0	1	10
SLT	0	1	11
NOR	1	1	00



Title

- Bullet