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Mike Parker

Professional Interests

My interests include computer architecture, performance analysis, and VLSI design. Past work includes reducing communication latency and overhead in clusters of workstations though efficient protocols and closely coupled network interface hardware, intelligent memory controller architecture and hardware design, and future generation DSM supercomputer architecture.

Education

Ph.D. Candidate, University of Utah, Advisor Dr. Al Davis. Expected graduation: December 2003

Dissertation Topic: *Improving I/O and Message-Passing Performance through Direct User-Level Event Notifications*

My dissertation research focuses on reducing message-passing and I/O overhead by exposing interrupt-like mechanisms directly to the user. Specifically, I am studying ways to enhance the performance of user-level "asynchronous branches" (e.g., user-level interrupts) in single threaded and SMT processors, and techniques for dynamically scheduling or creating event handling threads on SMT processors.

Bachelor of Science in Electrical Engineering, University of Oklahoma. May 1995

Publications

"Efficient Address Remapping in Distributed Shared-Memory Systems," Lixin Zhang, **Mike Parker**, John Carter. Submitted to HPCA 2004

"Active Memory Operations," Lixin Zhang, Zhen Fang, John B. Carter, **Mike Parker**. Submitted to Micro 2003

"ML-RSIM Reference Manual," Lambert Schaelicke, **Mike Parker**, Tech. Report 02-10, Department of Computer Science and Engineering, Univ. of Notre Dame, Notre Dame, Ind., 2002

"A Case for User-Level Interrupts," **Mike Parker**, HPCA Work-In-Progress, February 2002

"Message-Passing for the 21st Century: Integrating User-Level Networks with SMT," **Mike Parker**, Al Davis, Wilson Hsieh, Fifth Workshop on Multithreaded Execution, Architecture and Compilation, December 2001

"The Impulse Memory Controller," Lixin Zhang, Zhen Fang, **Mike Parker**, Binu K. Mathew, Lambert Schaelicke, John B. Carter, Wilson C. Hsieh, and Sally A. McKee, IEEE Transactions on Computers, Special Issue on Advances in High Performance Memory Systems, November 2001

"Impulse: Building a Smarter Memory Controller," J.B. Carter, W.C. Hsieh, L.B. Stoller, M.R. Swanson, L. Zhang, E.L. Brunvand, A. Davis, C.-C. Kuo, R. Kuramkote, **M.A. Parker**, L. Schaelicke, and T. Tateyama, Fifth International Symposium on High Performance Computer Architecture (HPCA-5), January 1999, pp. 70-79

"Memory System Support for Irregular Applications," J. Carter, W. Hsieh, M. Swanson, L. Zhang, A. Davis, **M. Parker**, L. Schaelicke, L. Stoller, and T. Tateyama, Fourth Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers (LCR '98), May 1998

"Interactive Ray Tracing for Volume Visualization," S. Parker, **M. Parker**. Y. Livnat, P.-P. Sloan, C. Hansen, and P. Shirley, IEEE Transactions on Visualization and Computer Graphics, July-September 1999

"Interacting with Gigabyte Volume Datasets on the Origin 2000," S. Parker, P. Shirley, Y. Livnat, C. Hansen, P.-P. Sloan, and **M. Parker**, The 41st Annual Cray User's Group Conference, 1999

"Efficient Communication Mechanisms for Cluster Based Parallel Computing," Al Davis, Mark Swanson, **Mike Parker**, Workshop on Communication and Architectural Support for Network-Based Parallel Computing, December 1996

Professional Experience

Research Staff, June 1999 - present
University of Utah, School of Computing, Dr. John Carter
SGI/DARPA HPCS Project (2002-2003)

As a part of the initial phases of the DARPA High-Productivity Computer Systems project, Silicon Graphics (SGI) investigated the inclusion of ideas from our Avalanche and Impulse research projects in future generation systems. Our Utah-based team cooperated with engineers from SGI, MIT, UMN, and GWU to architect large scale commercial DSM systems for the year 2010. As a prior researcher under both the Impulse and Avalanche projects, I helped extend and architect these ideas into a proposed future generation system. In addition, I investigated other architectural ideas and techniques to improve performance, reliability, and programmability.

Impulse research project (1999-2002)

The goal of the Impulse research project was to significantly reduce memory system overhead by improving cache and processor bus utilization on data intensive codes. Impulse provides a vector-like scatter/gather memory system to a conventional superscalar processor. I was responsible for the overall architecture of the memory controller and led the hardware prototyping effort. In addition to managing the hardware team and mentoring several masters and Ph.D. students, I designed pieces of the system, including the front-end to the scatter/gather address generator, the gather unit, and the I/O interfaces. I also maintained commercial CAD tools and developed additional design tools needed by the group. I played a significant role in the design and layout of the two versions of the system boards on which Impulse was tested.

VLSI and Hardware Engineer, August 1998 - June 1999
Phobos Corporation, Salt Lake City, Utah

I was originally recruited as a part-time employee/consultant to help move an FPGA implementation of an Ethernet MAC into an ASIC. As that project developed, I also researched and helped develop and prototype initial hardware designs of a high-end corporate network switch product. I designed a large FPGA based node board and developed Verilog designs as a part of the early hardware and software prototype system. I declined positions as both a hardware engineer and as the VP of engineering to continue work on my doctorate.

Research Assistant, December 1995 - June 1999
University of Utah, Department of Computer Science, Drs. Al Davis and John Carter
Avalanche and Impulse research projects

I helped develop architectural simulators and used these simulators to research various message cache organization and design details. I designed, simulated, and synthesized behavioral and RTL components including a message-cache controller, a command queue, flash and I/O controllers,

and test interfaces. I helped specify, design, and layout a fully custom FIFO, an SRAM, and I/O pads. I assisted in ASIC place and route, clock-tree generation, timing closure, and tape-out design checks. I developed tools to place graphics on our ASICs and to aid in the testing and debugging of simulated, FPGA, and ASIC designs used in the projects. Furthermore, I participated in the schematic capture and layout of printed circuit boards used to test designs developed in this project. I modified the OS and developed applications to test our FPGA and ASIC designs. I also installed and maintained commercial CAD tools for use by the project.

Teaching Assistant, September 1995 - December 1995
University of Utah, Department of Computer Science
Fundamentals of VLSI Design

Assisted in teaching and developing labs to teach ASIC layout and design tool use.

Software Engineer / Systems Administrator, August 1992 - August 1995
University of Oklahoma, Department of Aerospace and Mechanical Engineering

I managed a network of Sun SPARC workstations, with approximately 70 user accounts. I was responsible for systems administration, user support, and software development.

System administration and software development consulting, 1993-1995
YKS International, Dr. Ajay Agrawal, Dr. Sam Lee, Dr. Joe Bastian, and Dr. Ron Cox

I performed system administration, software development and hardware development tasks.

Physics Undergraduate Research Assistant, 1989 - 1990
University of Oklahoma, Department of Physics and Astronomy

I numerically determined solutions to Schrödinger's equations, and translated and rewrote older Fortran code into Fortran 77.

Skills

My specialties are in computer architecture, simulation systems, memory systems, I/O systems and processor design. I have experience that allows me to approach architecture both from a low-level hardware perspective as well as from a high-level software, compiler, and operating systems perspective.

I have experience in simulator development, architectural modeling and evaluation, hardware design, application porting and development, operating system development, and device driver writing. I have designed significant hardware using both VHDL and Verilog at the behavioral, RTL and gate levels. I have experience with custom layout, standard cell design, spice, DRC, ERC, LVS and tape-out. I have been involved in the architecture, design, and testing of both semi-custom and standard cell chips in 1.2µm, 0.5µm, 0.25µm, and 0.18µm CMOS technologies, including a semi-custom 100 mm^2 cluster communication interface test chip operating at 133 MHz in 0.5µm CMOS. I have experience in schematic capture and high-speed circuit board layout.

CAD tool experience: Synopsys VSS, VCS, Design Compiler, Module Compiler, and FPGA Compiler; Cadence Design Planner, Ambit, DSM Silicon Ensemble, CTGen, Virtuoso, Diva, Dracula, Spectre, Allegro, Advanced Package Designer, Specctra, and OrCAD, Duet Technologies Epoch and TACTIC, Avant! Hspice, Viewlogic Powerview, Espresso and other associated tools.

Programming languages: VHDL, Verilog, Verilog PLI, C, C++, Java, Pascal, Fortran, BASIC, various assembly languages, various shell and scripting languages

Honors

Eta Kappa Nu Electrical Engineering Honor Society

Golden Key National Honor Society

Dean's Honor Roll, College of Engineering, University of Oklahoma

Other Awards

"Multiprocessor Digital Signal Processing Flow Velocity Analyzer," with Travis D. Fox, 1994; won award for exceptional project in Digital Design class, University of Oklahoma

"The Exploding Disk," with Travis D. Fox, 1993; won award for exceptional project in display for Engineering Open House, University of Oklahoma

Activities

Held several leadership positions both professionally and as a volunteer:

Computer Policy Committee, CS Dept., Univ. of Utah, 1998-2001

Future of the Department Committee, CS Dept., Univ. of Utah, 1999

Graduate Student Advisory Committee, CS Dept., Univ. of Utah, 1996-1999

IEEE University of Oklahoma Chapter Vice President, 1994-1995

IEEE Display Committee Chair, Univ. of Oklahoma, 1993

Other Service

Electronics CAD tools maintenance, College of Engr., Univ. of Utah, 1998-present

Graduate Student Recruiting Activities, CS Dept., Univ. of Utah, 1996-present

Faculty Recruiting Activities, CS Dept., Univ. of Utah, 1996-present

Ph.D. Comprehensive Exam reviews, CS Dept., Univ. of Utah, 1997-1999

Primary Children's Medical Center Volunteer, 1996-1997

Served a mission for the Church of Jesus Christ of Latter-day Saints, 1990-1992

Several other volunteer church positions, including leadership and teaching positions

References

Dr. John Carter	retrac@cs.utah.edu	801-585-5474
Dr. Al Davis	ald@cs.utah.edu	801-581-3991
Dr. Wilson Hsieh	wilson@cs.utah.edu	801-585-5047
Dr. Erik Brunvand	elb@cs.utah.edu	801-581-4345
Dr. Sally McKee	sam@csl.cornell.edu	607-255-2672
Dr. Ganesh Gopalakrishnan	ganesh@cs.utah.edu	801-581-3568

Professional Memberships

ACM Member since 1998

IEEE Member since 1992