

Chapter 7

Spectre Analog Simulator

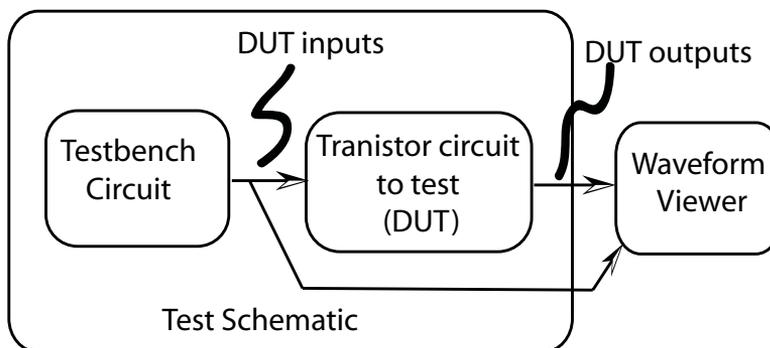
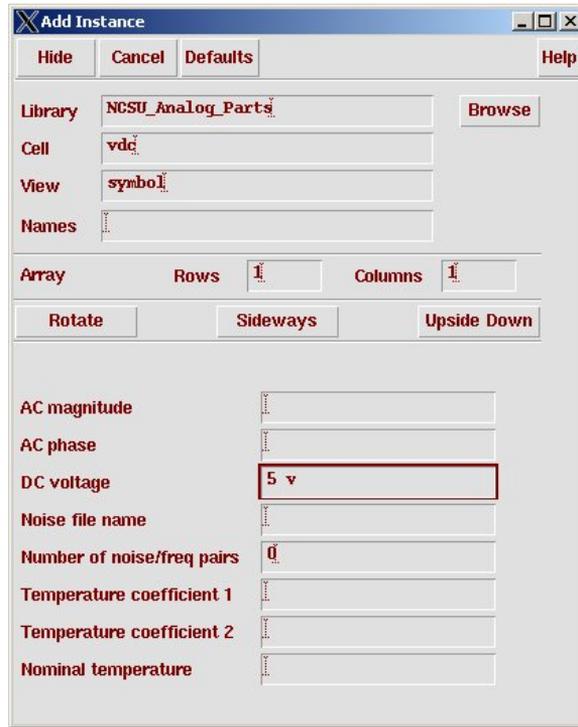


Figure 7.1: The analog simulation environment for a circuit (DUT)



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Figure 7.2: Component parameters for the vdc voltage source

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To

Show system user CDF

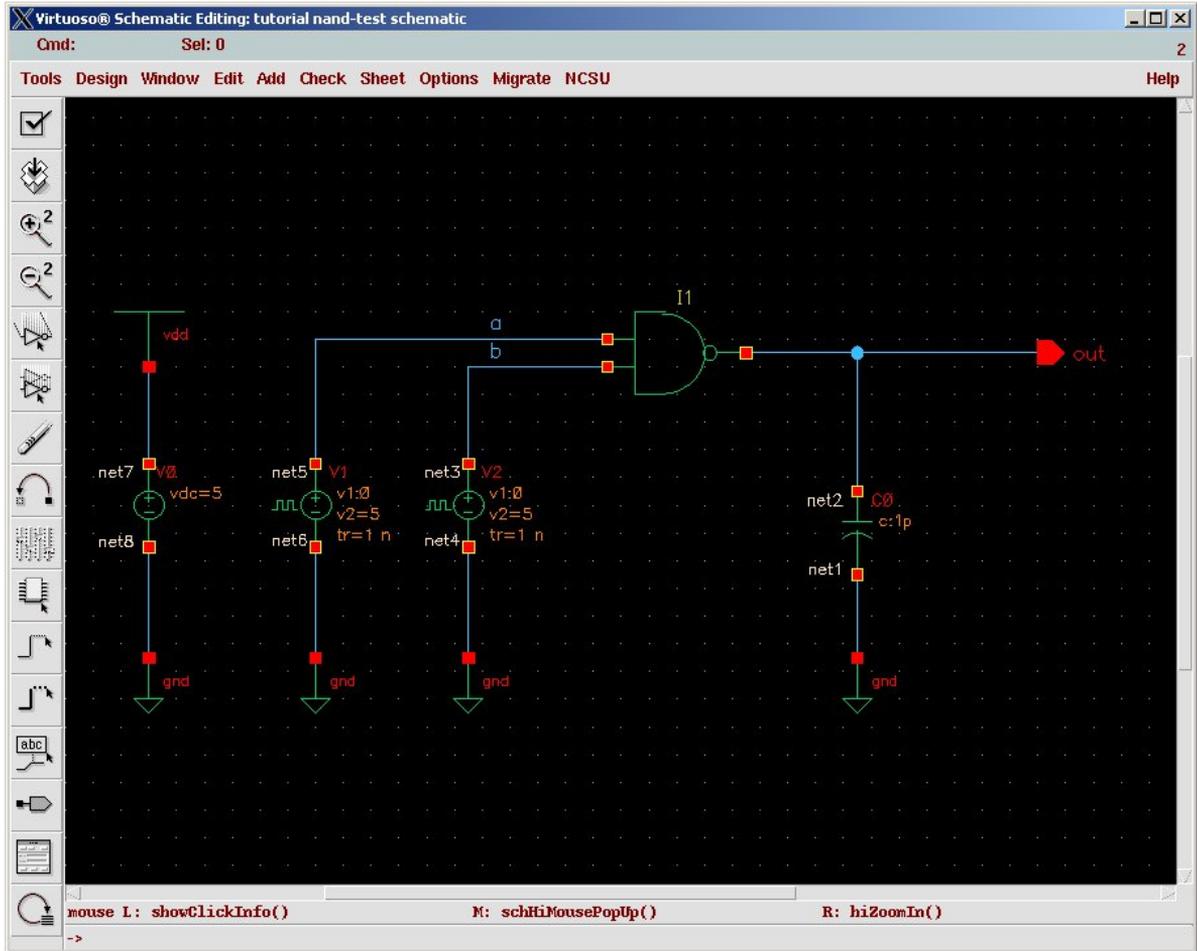
Property	Value	Display
Library Name	NCSU_Analog_Parts	off
Cell Name	vpulse	off
View Name	symbol	off
Instance Name	V1	off

User Property	Master Value	Local Value	Display
Ivignore	TRUE		off

CDF Parameter	Value	Display
AC magnitude		off
AC phase		off
Voltage 1	0 V	off
Voltage 2	5 V	off
Delay time	0 s	off
Rise time	1n s	off
Fall time	1n s	off
Pulse width	10n s	off
Period	20n s	off
DC voltage		off
Noise file name		off
Number of noise/freq pairs	0	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off

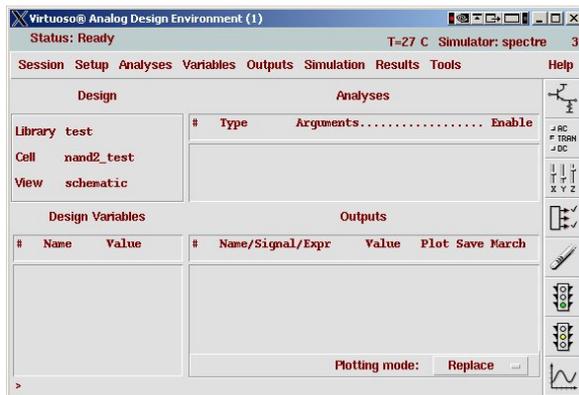
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Figure 7.3: Component parameters for the `vpulse` voltage source



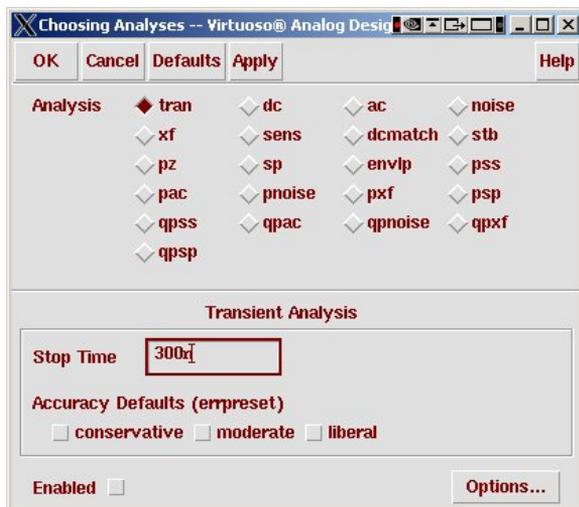
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Figure 7.4: Schematic for the nand-test DUT/testbench circuit



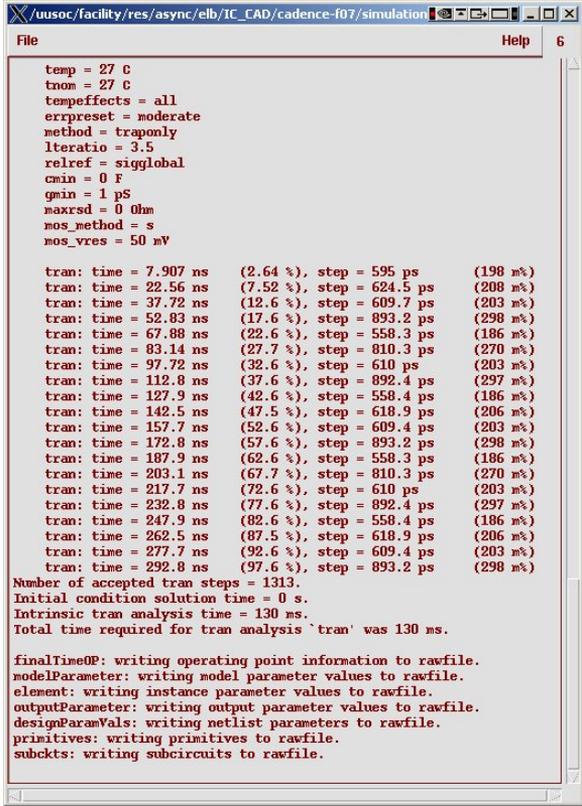
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Figure 7.5: Virtuoso Analog Environment control window



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Figure 7.6: Choosing Analyses dialog box



```

/uusoc/facility/res/async/elb/IC_CAD/cadence-f07/simulation
File Help 6

temp = 27 C
tnom = 27 C
tempeffects = all
errpreset = moderate
method = trapezoid
lteratio = 3.5
relref = sigglobal
cmin = 0 F
gmin = 1 pS
maxrsd = 0 Ohm
nos_method = s
nos_vres = 50 mV

tran: time = 7.907 ns (2.64 %), step = 595 ps (198 m%)
tran: time = 22.56 ns (7.52 %), step = 624.5 ps (208 m%)
tran: time = 37.72 ns (12.6 %), step = 609.7 ps (203 m%)
tran: time = 52.83 ns (17.6 %), step = 893.2 ps (298 m%)
tran: time = 67.88 ns (22.6 %), step = 558.3 ps (186 m%)
tran: time = 83.14 ns (27.7 %), step = 810.3 ps (270 m%)
tran: time = 97.72 ns (32.6 %), step = 610 ps (203 m%)
tran: time = 112.8 ns (37.6 %), step = 892.4 ps (297 m%)
tran: time = 127.9 ns (42.6 %), step = 558.4 ps (186 m%)
tran: time = 142.5 ns (47.5 %), step = 618.9 ps (206 m%)
tran: time = 157.7 ns (52.6 %), step = 609.4 ps (203 m%)
tran: time = 172.8 ns (57.6 %), step = 893.2 ps (298 m%)
tran: time = 187.9 ns (62.6 %), step = 558.3 ps (186 m%)
tran: time = 203.1 ns (67.7 %), step = 810.3 ps (270 m%)
tran: time = 217.7 ns (72.6 %), step = 610 ps (203 m%)
tran: time = 232.8 ns (77.6 %), step = 892.4 ps (297 m%)
tran: time = 247.9 ns (82.6 %), step = 558.4 ps (186 m%)
tran: time = 262.5 ns (87.5 %), step = 618.9 ps (206 m%)
tran: time = 277.7 ns (92.6 %), step = 609.4 ps (203 m%)
tran: time = 292.8 ns (97.6 %), step = 893.2 ps (298 m%)

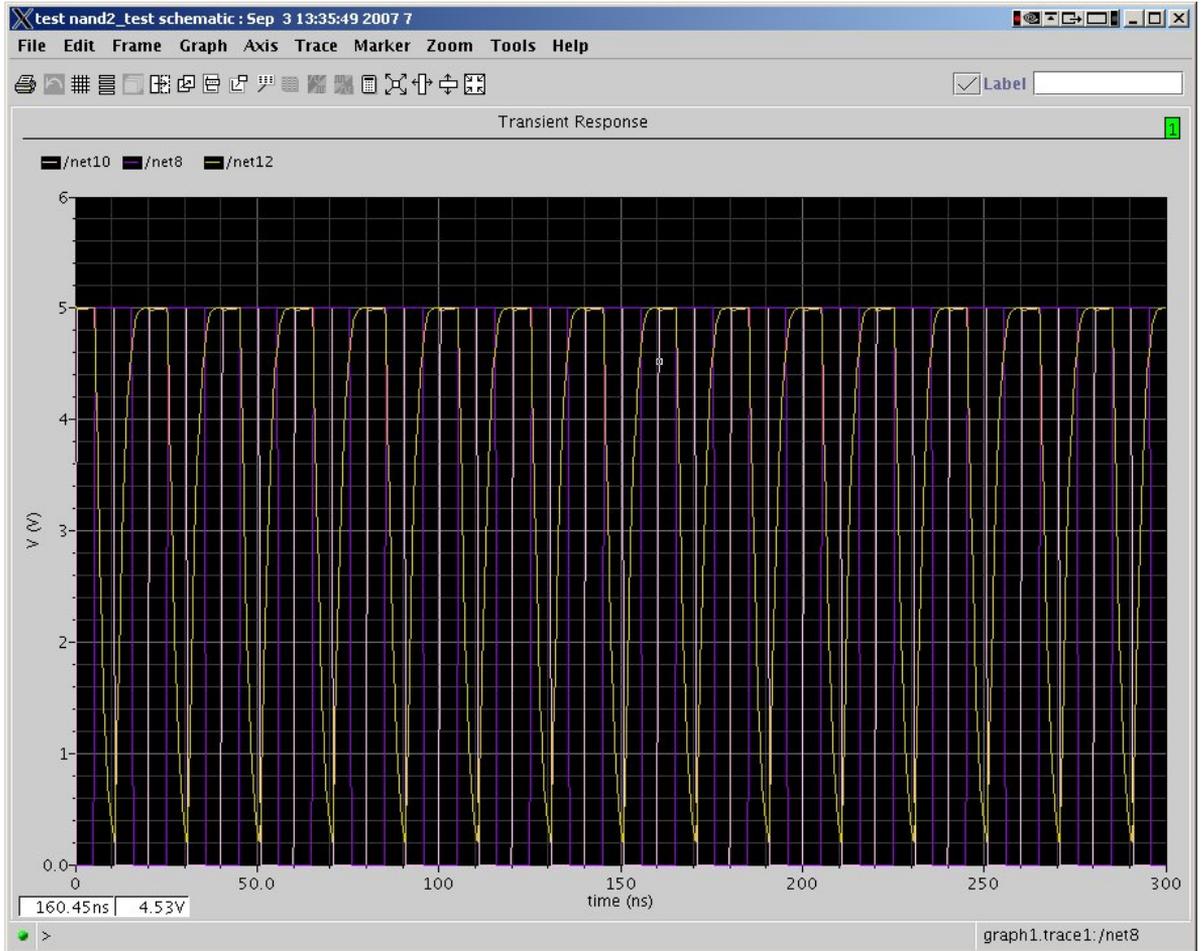
Number of accepted tran steps = 1313.
Initial condition solution time = 0 s.
Intrinsic tran analysis time = 130 ns.
Total time required for tran analysis `tran' was 130 ns.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.

```

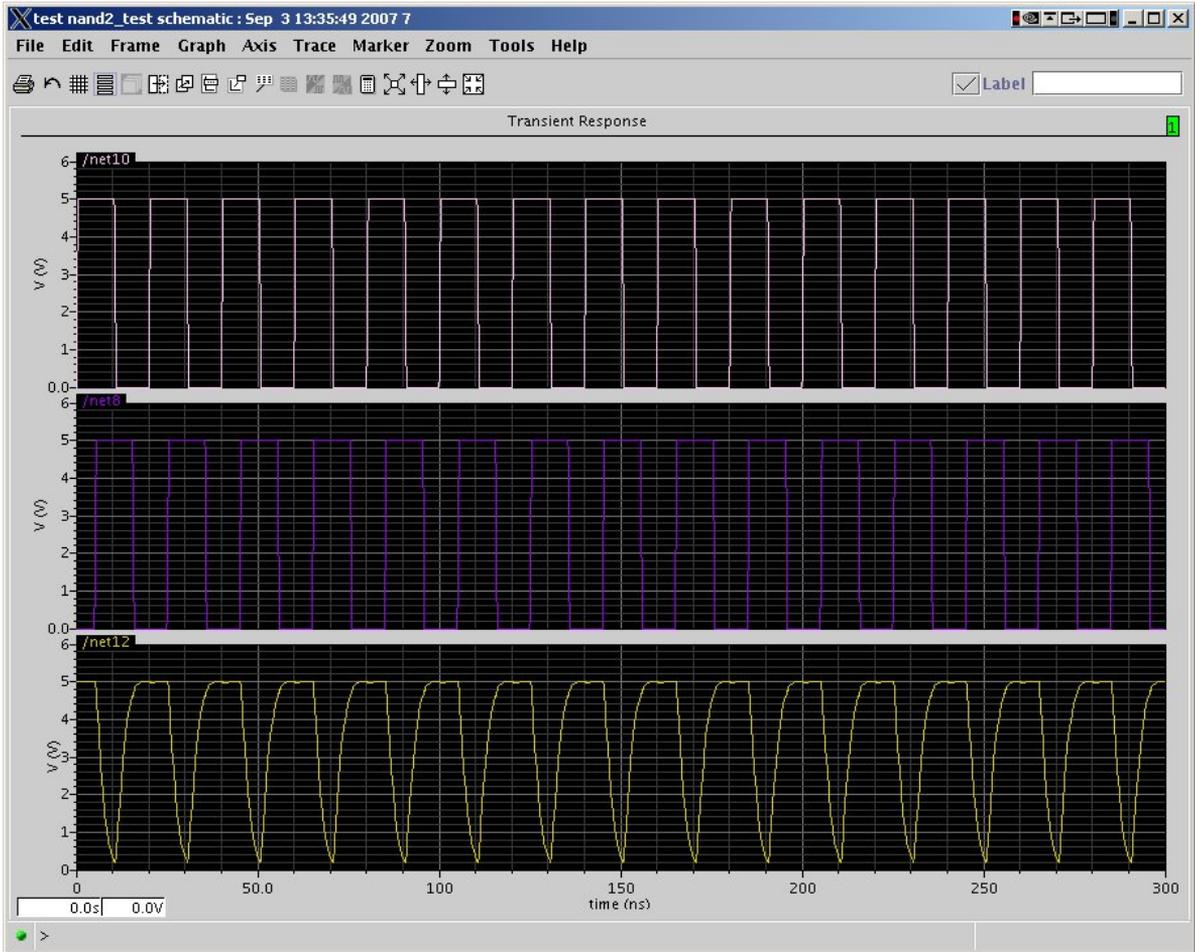
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Figure 7.7: Spectre log window for the NAND simulation



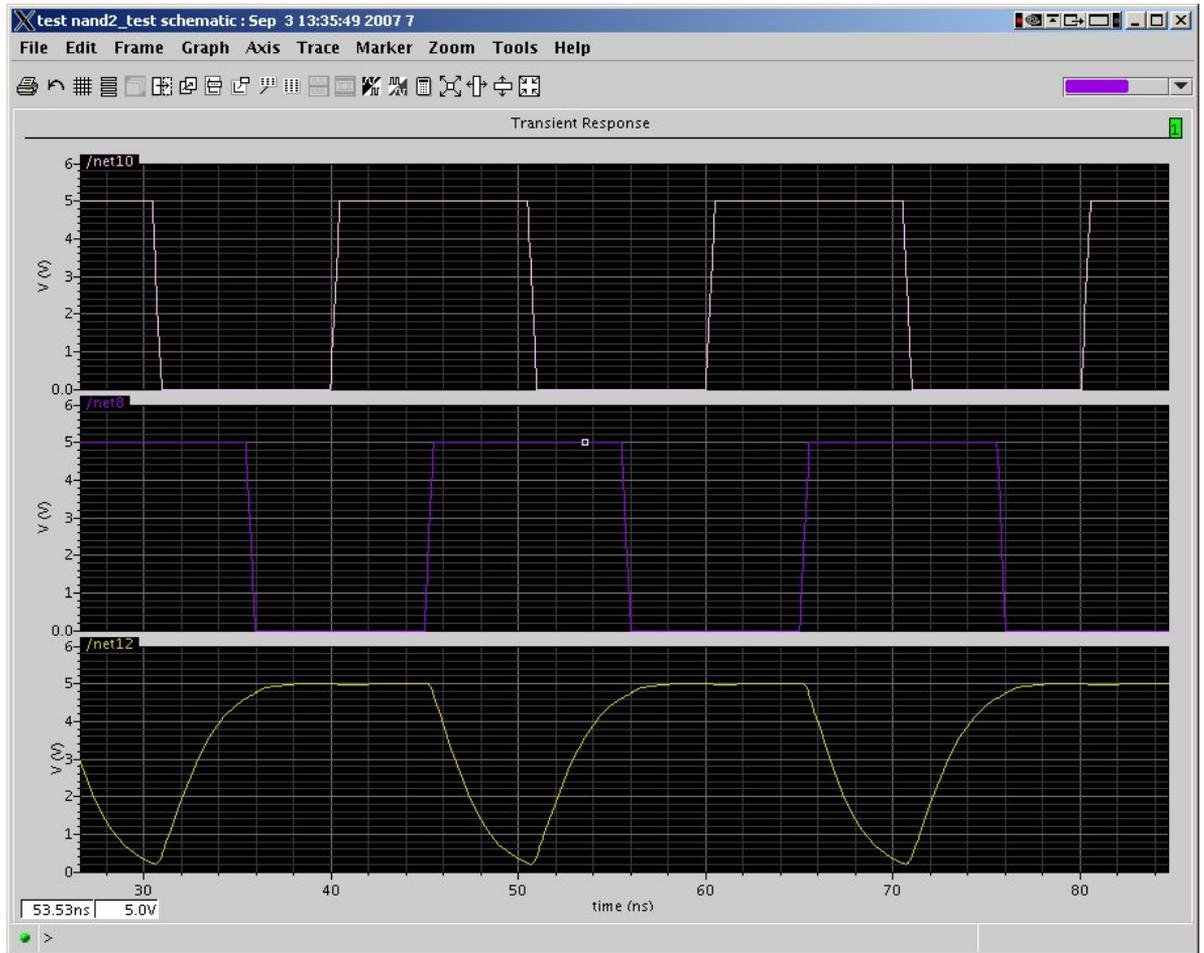
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Figure 7.8: Initial waveform output window



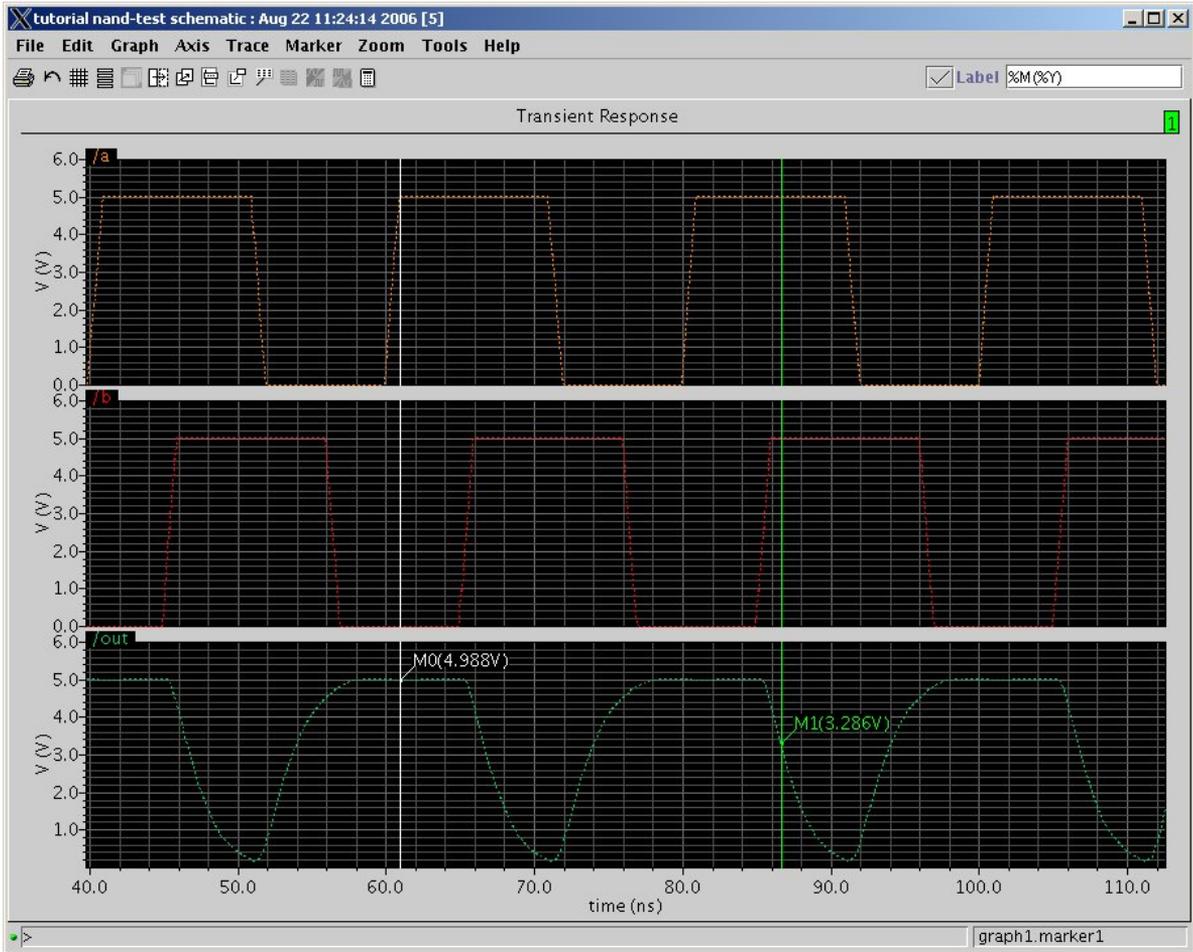
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Figure 7.9: Waveform output window in strip mode



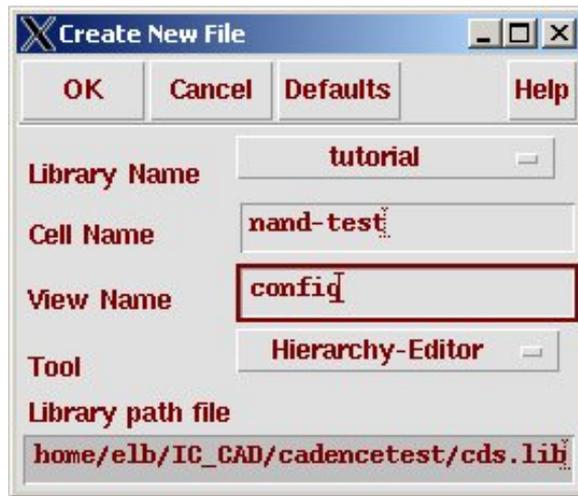
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Figure 7.10: Waveform output window: zoomed view



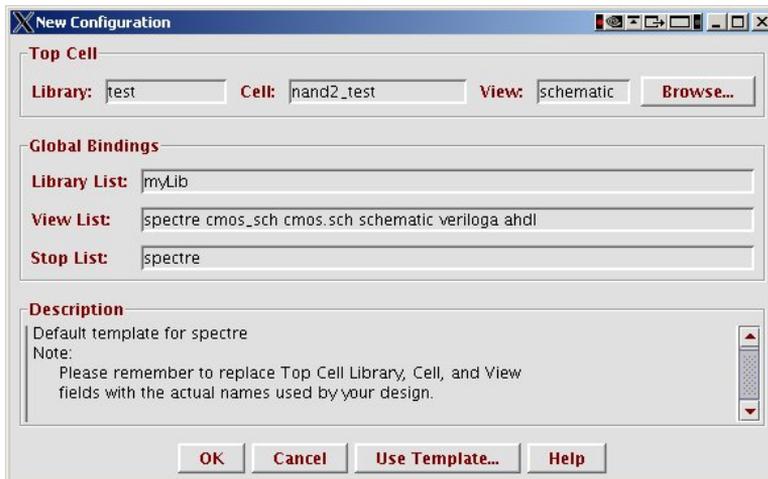
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Figure 7.11: Waveform output with markers



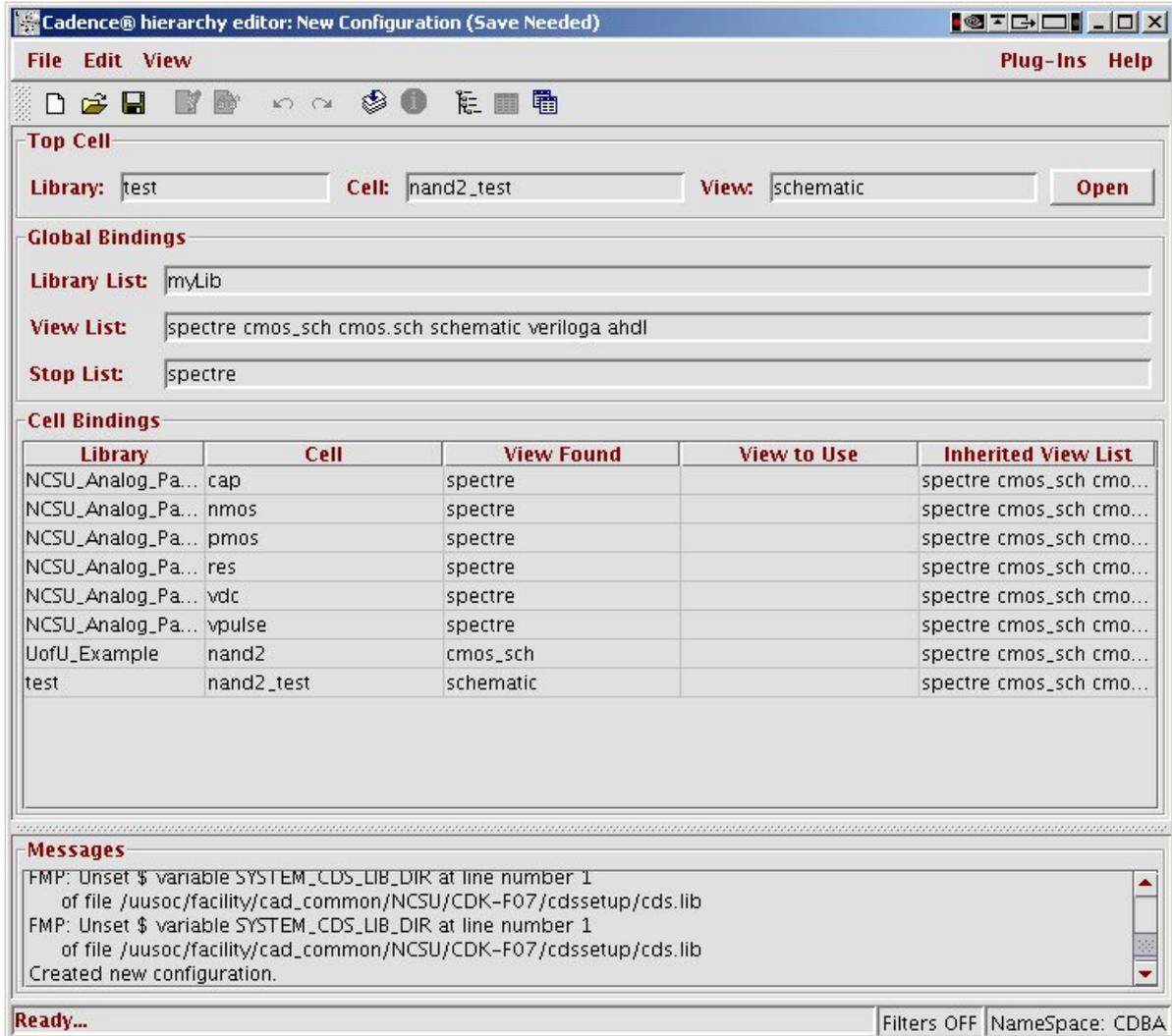
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Figure 7.12: Create New File dialog for the config view



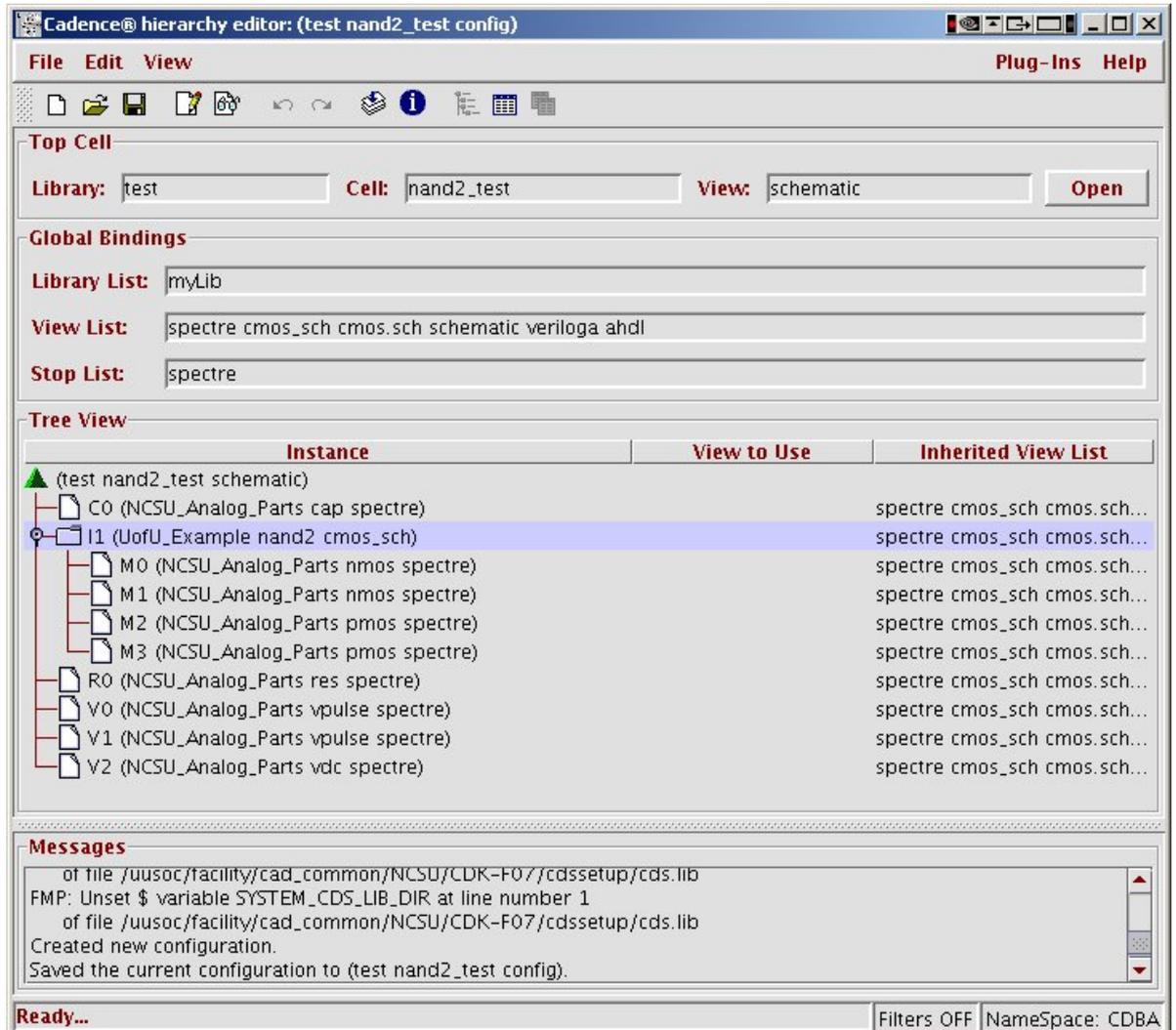
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Figure 7.13: New Configuration dialog box



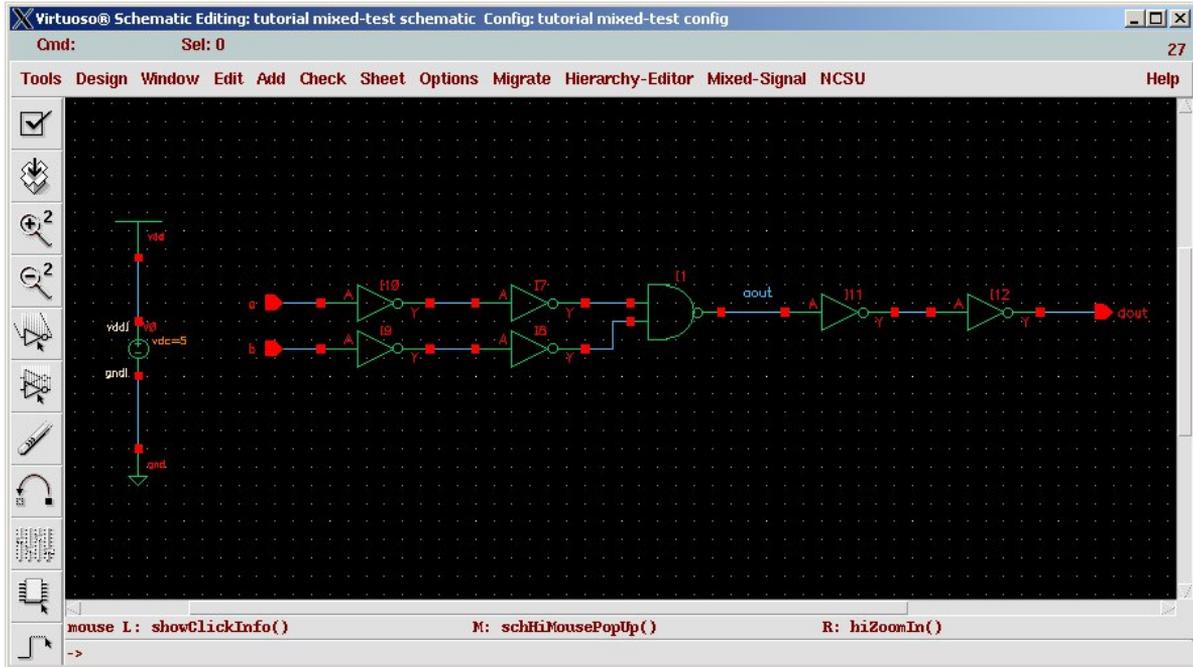
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Figure 7.14: Hierarchy Editor view for nand-test (table view)



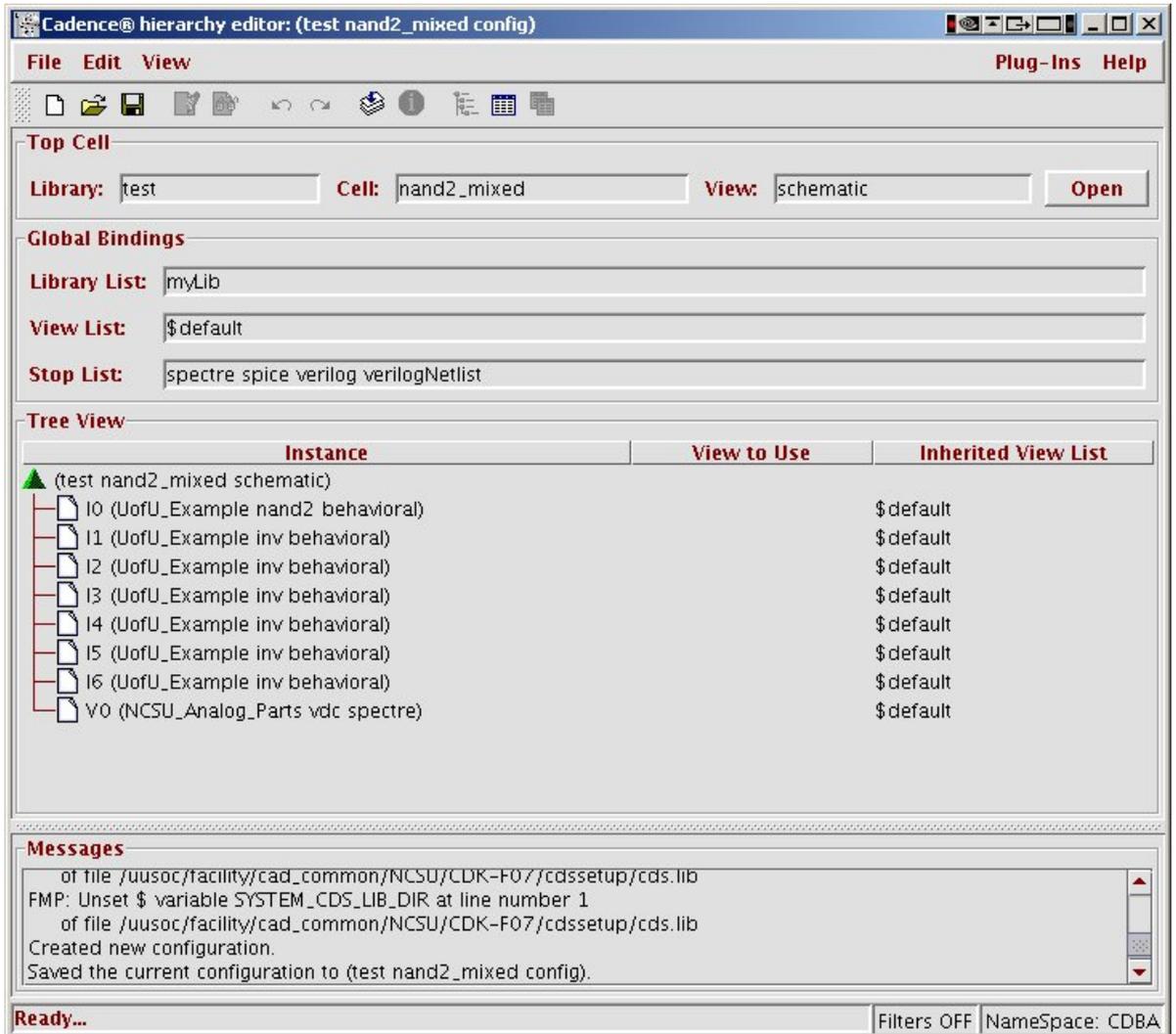
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Figure 7.15: Hierarchy Editor view for **nand-test** (tree view)



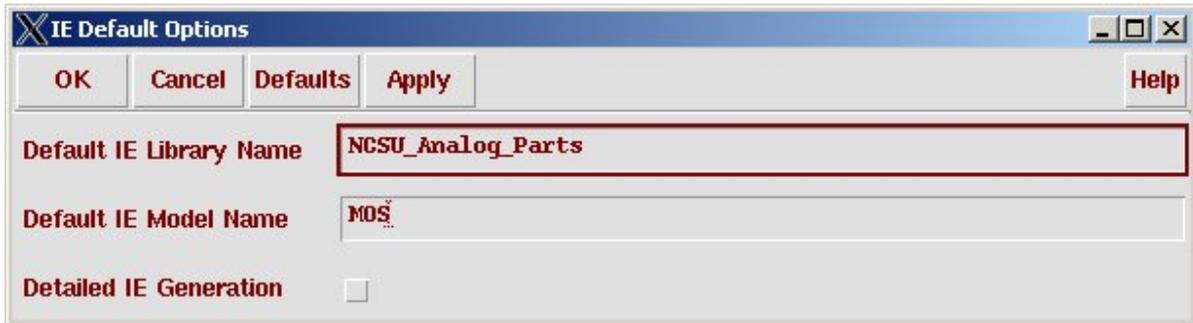
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Figure 7.16: Test schematic for the mixed-mode NAND (DUT) simulation



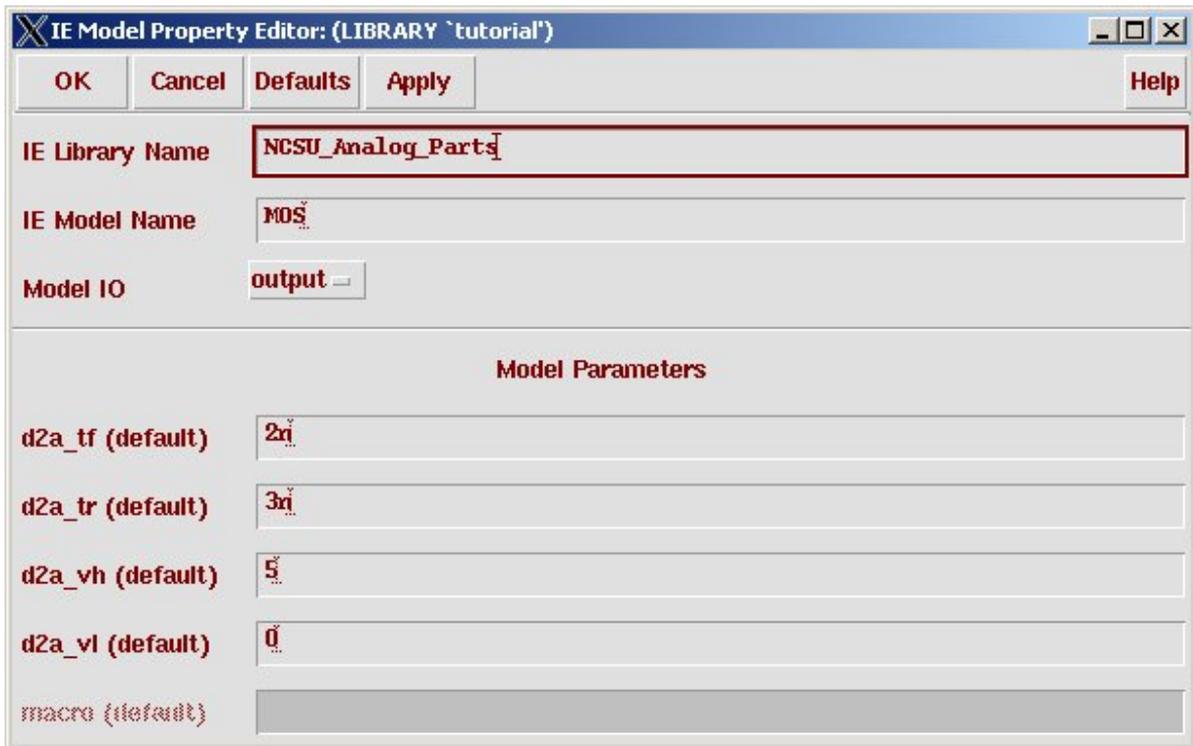
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Figure 7.17: Mixed-mode config view for mixed-nand



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Figure 7.18: Interface library dialog box



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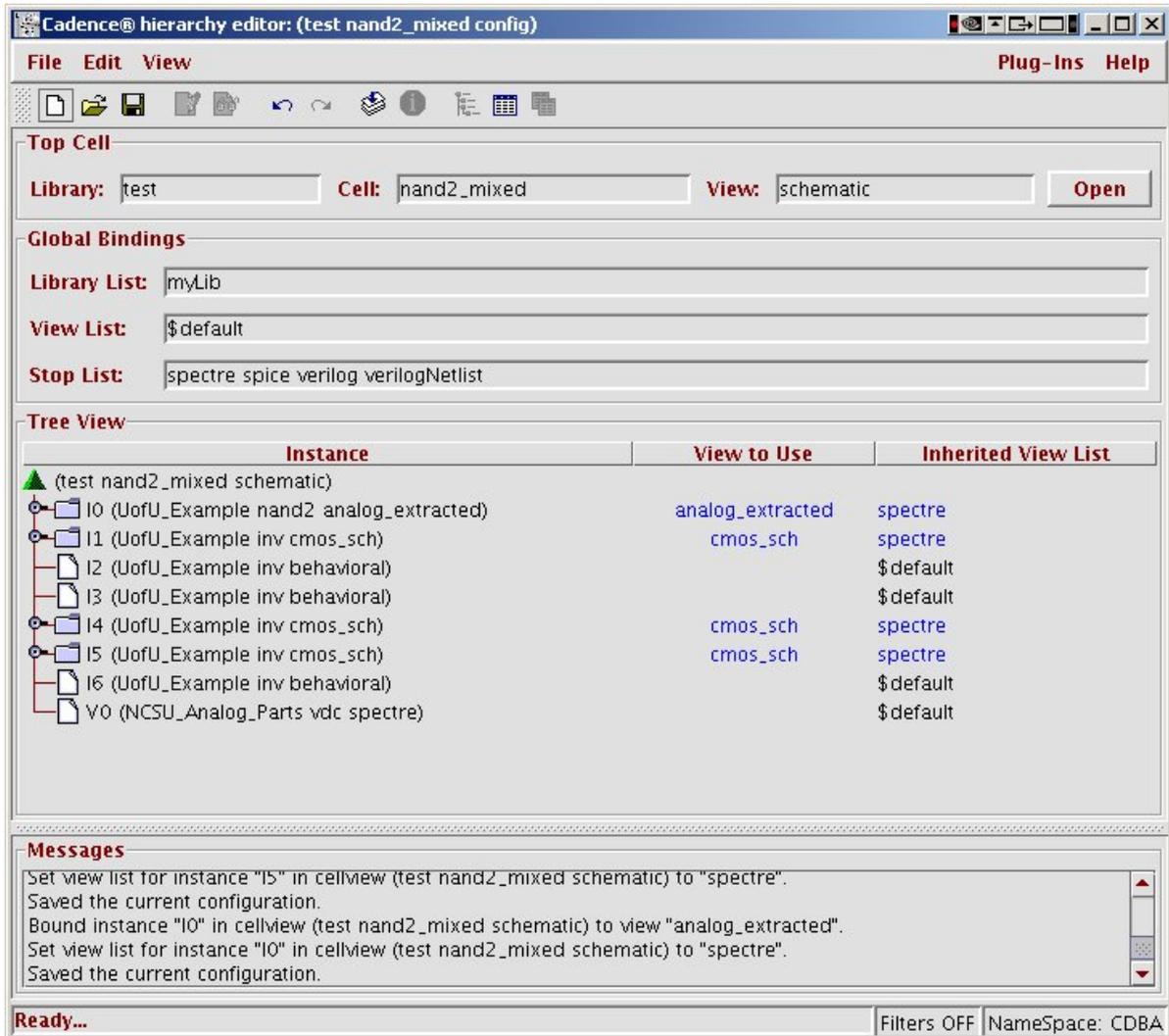
Figure 7.19: d2a interface element parameters

The image shows a software dialog box titled "IE Model Property Editor: (LIBRARY `tutorial')". It has a standard Windows-style title bar with minimize, maximize, and close buttons. Below the title bar are four buttons: "OK", "Cancel", "Defaults", and "Apply", followed by a "Help" button on the right. The main area of the dialog is divided into several sections:

- IE Library Name:** A text field containing "NCSU_Analog_Parts".
- IE Model Name:** A text field containing "MOS".
- Model IO:** A dropdown menu currently set to "input".
- Model Parameters:** A section header followed by four parameter fields:
 - a2d_tx (default):** A text field containing "1m".
 - a2d_v0 (default):** A text field containing "1.5".
 - a2d_v1 (default):** A text field containing "3.5".
 - macro (default):** An empty text field.

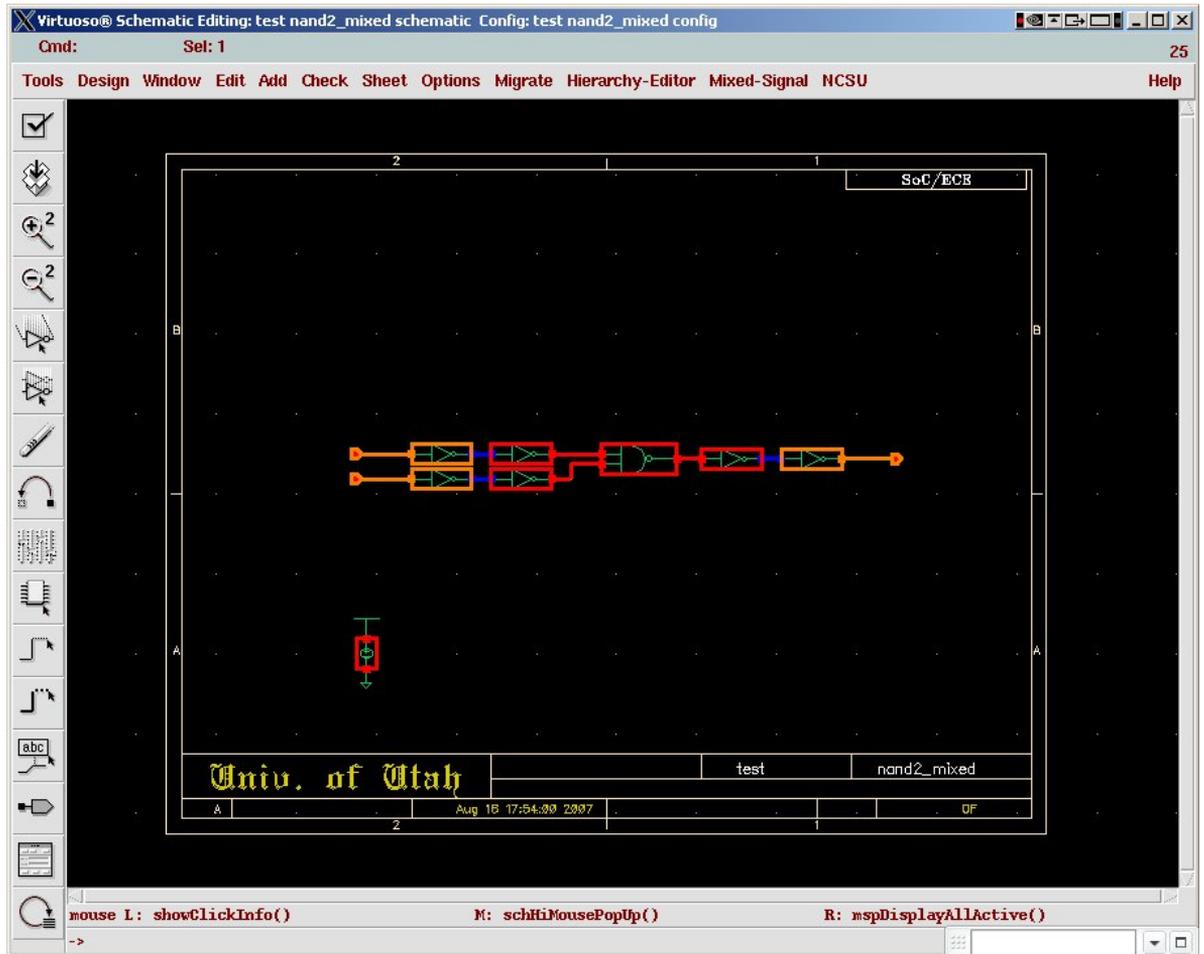
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Figure 7.20: a2d interface element parameters



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Figure 7.21: Mixed-mode config view with analog/Verilog partitioning



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Figure 7.22: The **mixed-test** schematic showing analog/digital partitioning

```
// Verimix stimulus file.
// Default verimix stimulus.

initial
begin

    a = 1'b0;
    b = 1'b0;

    #10 $display("ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $display("Error - that's wrong!");

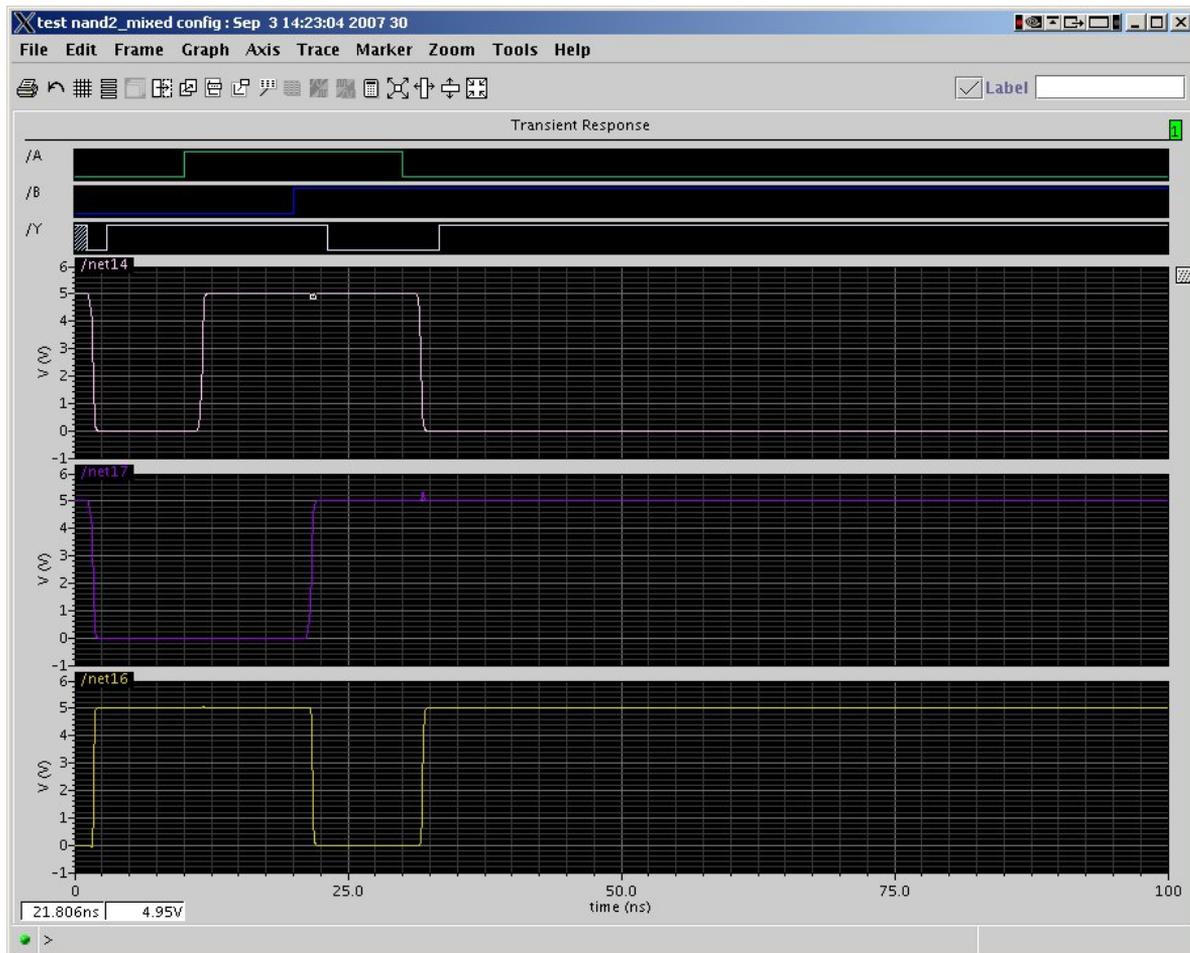
    a=1;
    #10 $display("ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $display("Error - that's wrong!");

    b=1;
    #10 $display("ab = %b%b, out = %b", a, b, dout);
    if (dout != 0) $display("Error - that's wrong!");

    a=0;
    #10 $display("ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $display("Error - that's wrong!");

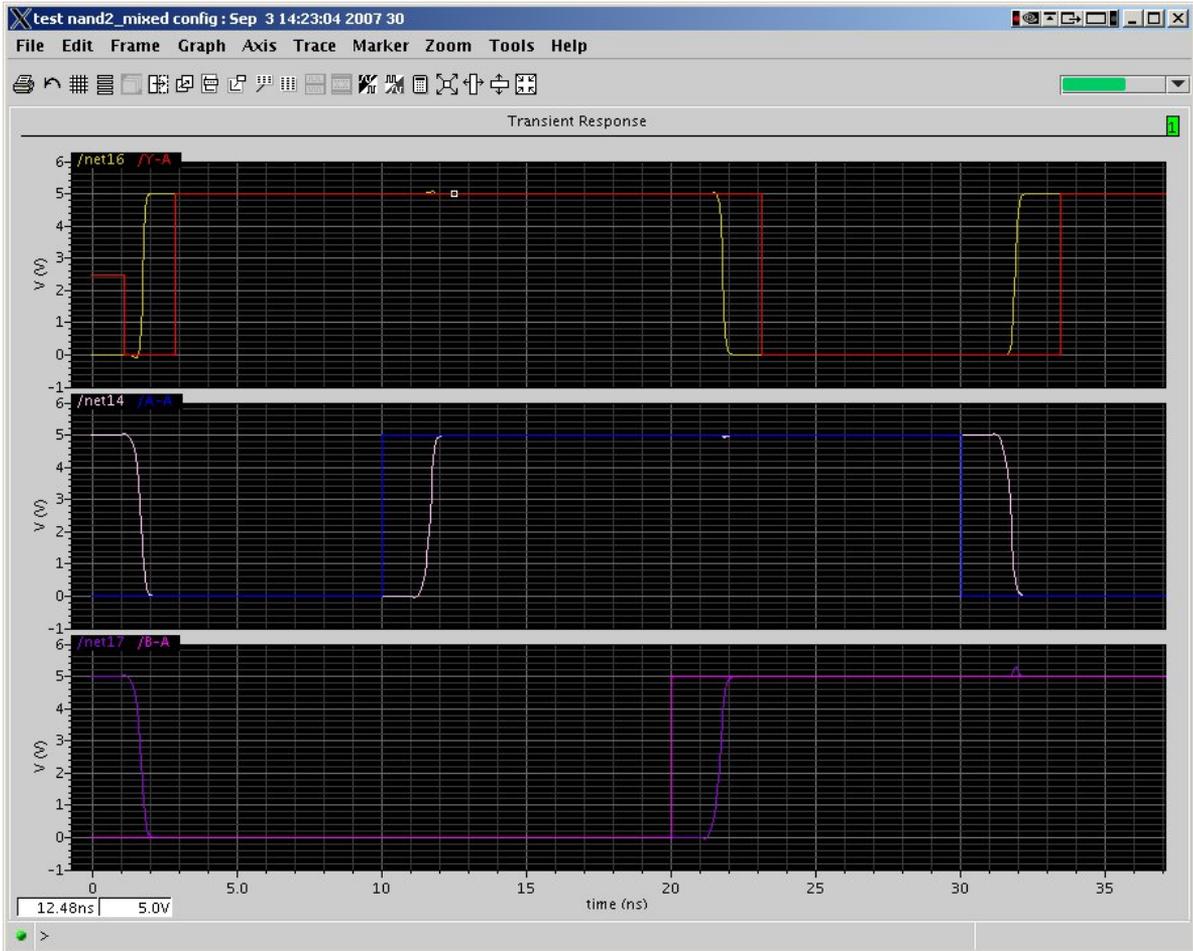
end
```

Figure 7.23: The digital testbench for the mixed-nand simulation



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Figure 7.24: Results of the mixed-mode simulation of **mixed-test**



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Figure 7.25: Rearranged results of the mixed-mode simulation

```

Switching from DC to transient.
VERILOG time 0 (units of 100ps) corresponds to spectre time 0.

Message!  At the end of DC initialization the logic values
          of the following ports are X (unknown):

          net16
          net18

                                     [Mixed_Sig]
          "IE.verimix", 4: ...
ab = 00, out = 1
ab = 10, out = 1
ab = 11, out = 0
ab = 01, out = 1
Verilog/spectre Interface: 165 messages sent, 167 messages received.
0 simulation events
(use +profile or +listcounts option to count) + 29 accelerated events
CPU time: 0.0 secs to compile + 0.0 secs to link + 3.6 secs in simulation
End of Tool:   VERILOG-XL       05.81.001-p   Aug 23, 2006  10:58:39

```

Figure 7.26: \$display output from the mixed-test simulation

```

// Verimix stimulus file.
// Default verimix stimulus.

integer file; // declare the file descriptor first
initial
begin
    file = $fopen("/home/elb/IC_CAD/cadencetest/testout.txt");
    a = 1'b0;
    b = 1'b0;

    $fdisplay(file, "Starting mixed-test simulation of NAND");
    $fdisplay(file, "using digital inputs to an analog simulation");

    #10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $fdisplay(file, "Error - that's wrong!");

    a=1;
    #10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $fdisplay(file, "Error - that's wrong!");

    b=1;
    #10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
    if (dout != 0) $fdisplay(file, "Error - that's wrong!");

    a=0;
    #10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
    if (dout != 1) $fdisplay(file, "Error - that's wrong!");

end

```

Figure 7.27: mixed-test testbench file with file I/O

```
Starting mixed-test simulation of NAND
using digital inputs to an analog simulation
ab = 00, out = 1
ab = 10, out = 1
ab = 11, out = 0
ab = 01, out = 1
```

Figure 7.28: mixed-test testbench file with file I/O

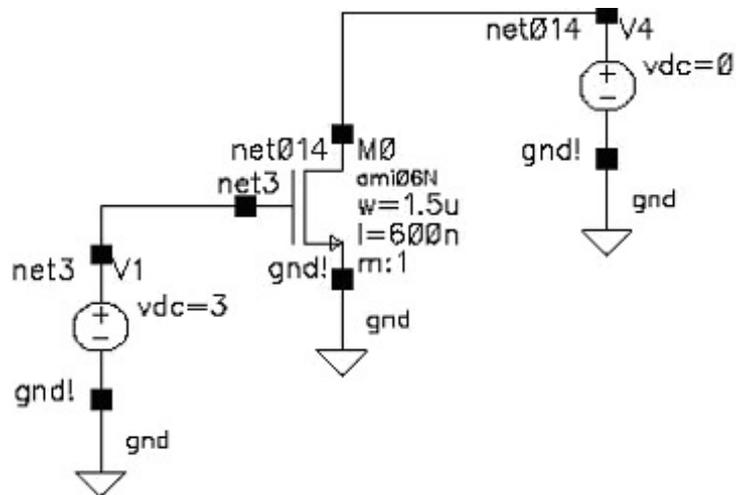
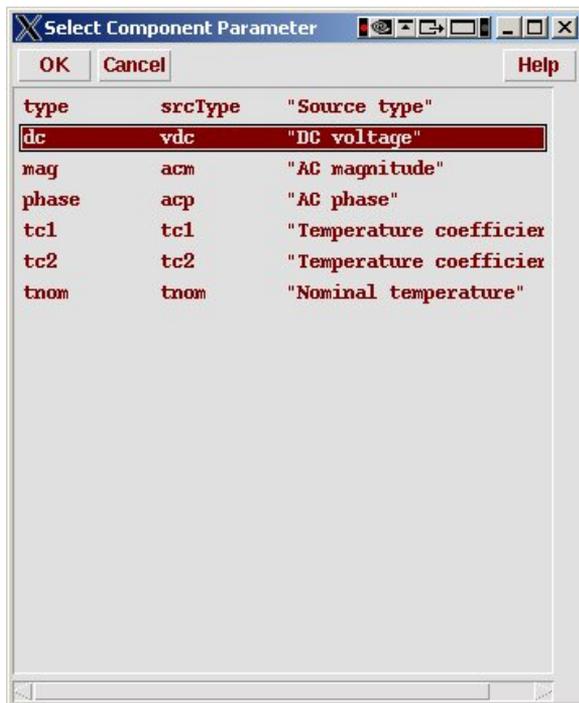
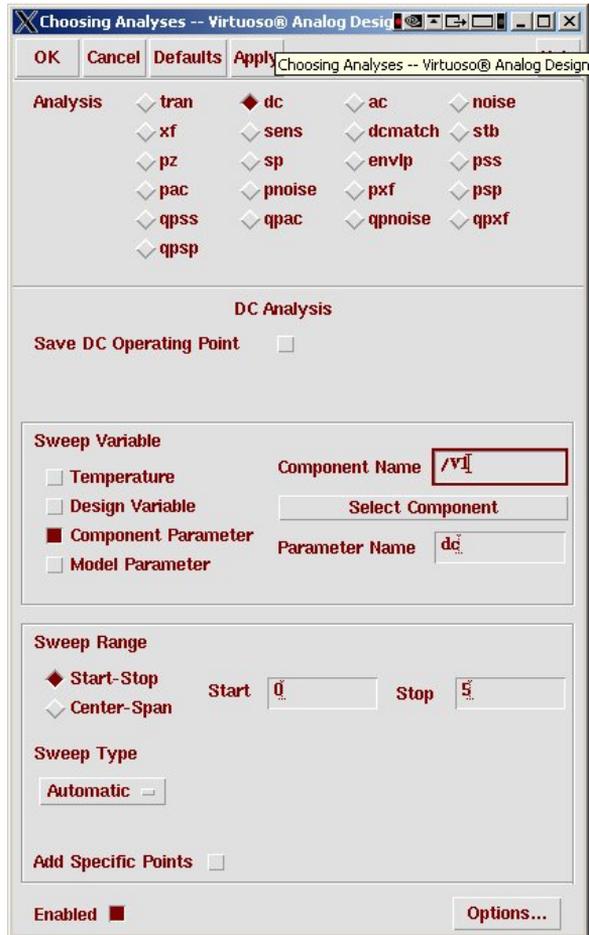


Figure 7.29: Simple circuit for DC analysis (schematic view)



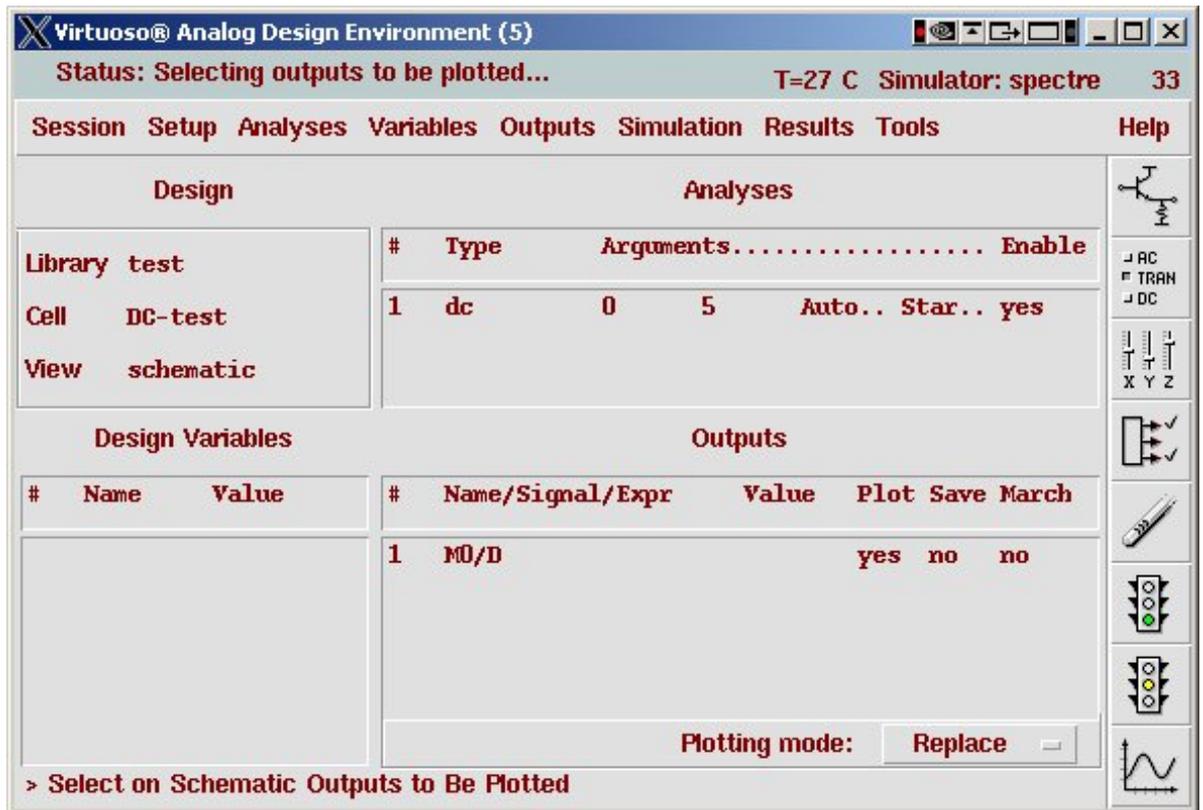
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Figure 7.30: Component parameter selection dialog box for DC analysis



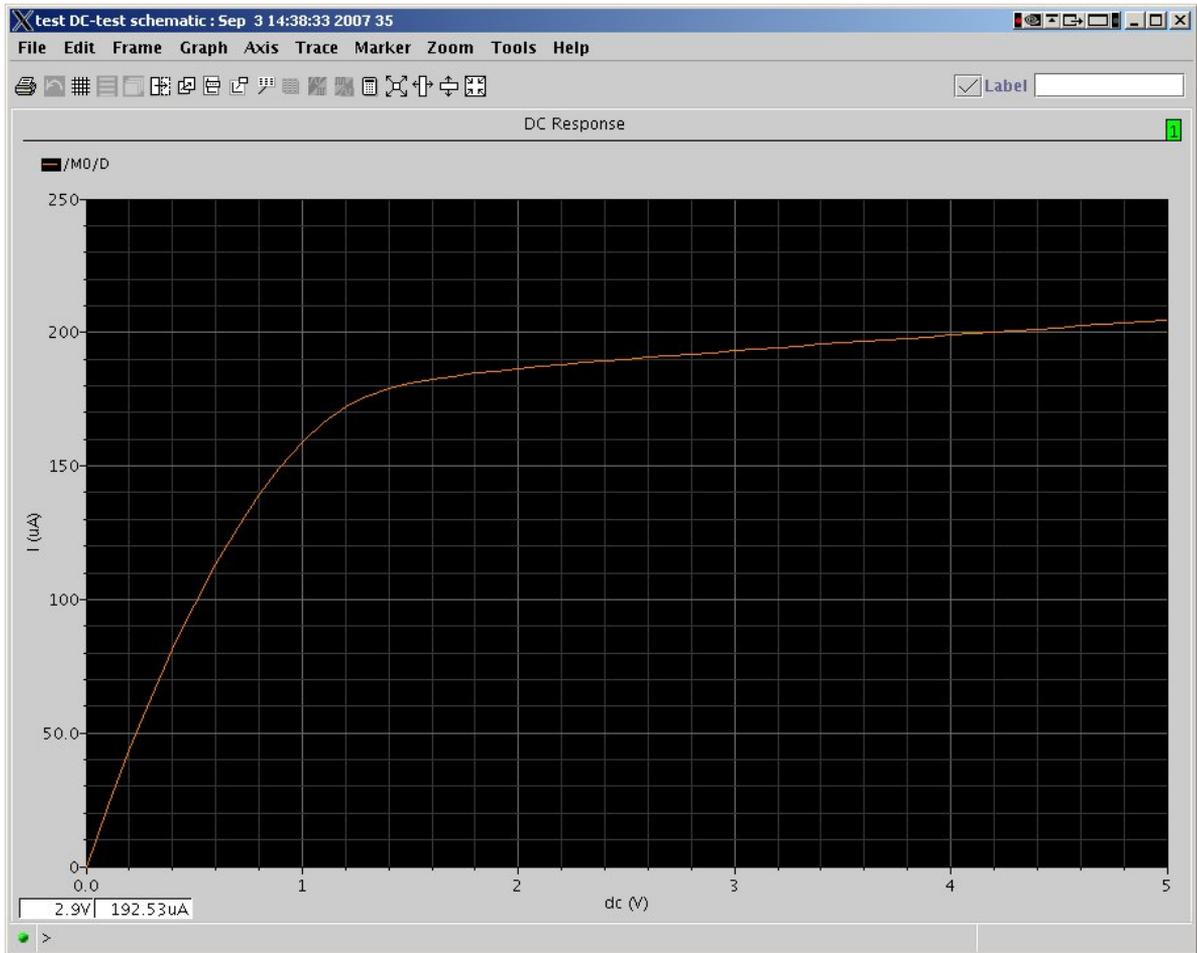
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Figure 7.31: DC analysis dialog box



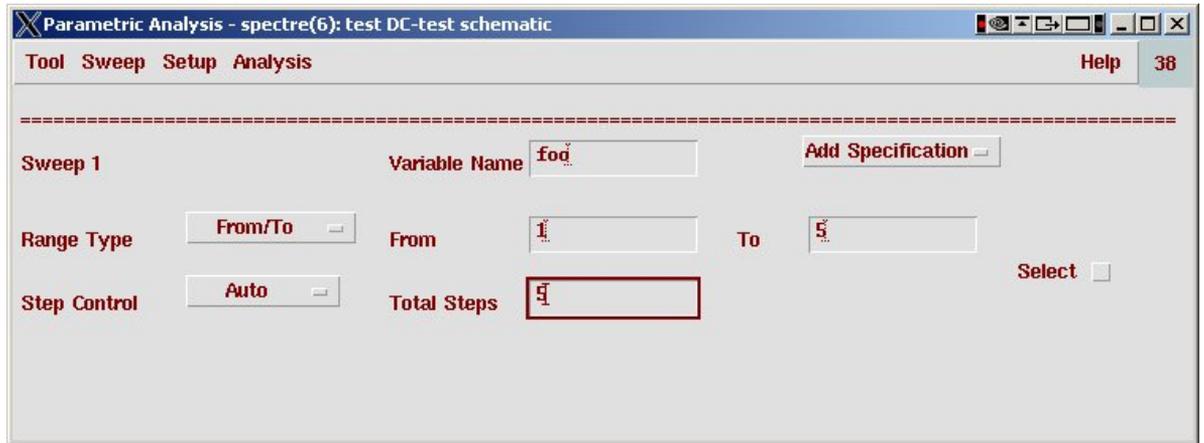
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Figure 7.32: Analog Environment dialog box for DC analysis



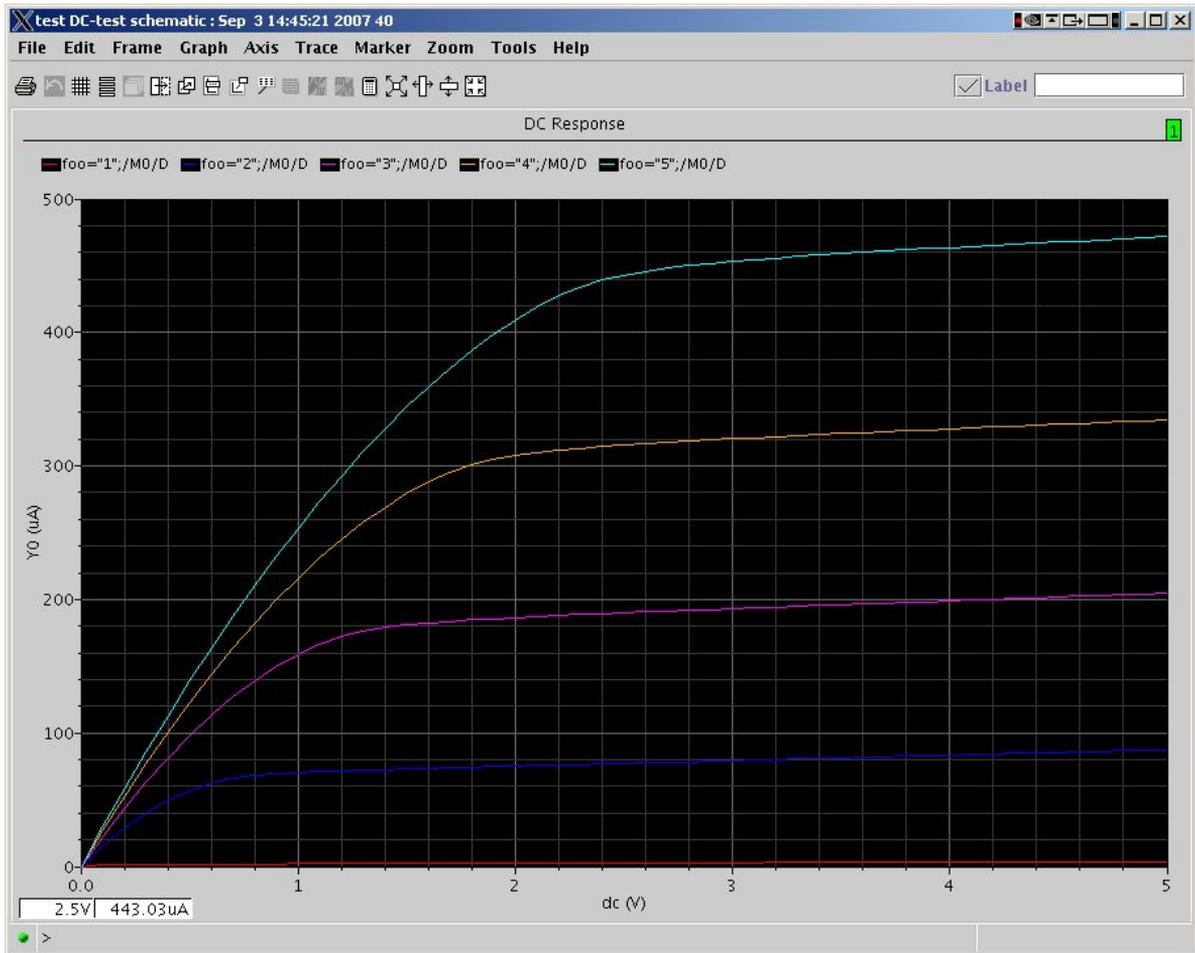
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Figure 7.33: DC analysis output waveform for a single set of parameters



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Figure 7.34: Dialog to set variable parameters for parametric simulation



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Figure 7.35: Output of parametric DC simulation with five curves

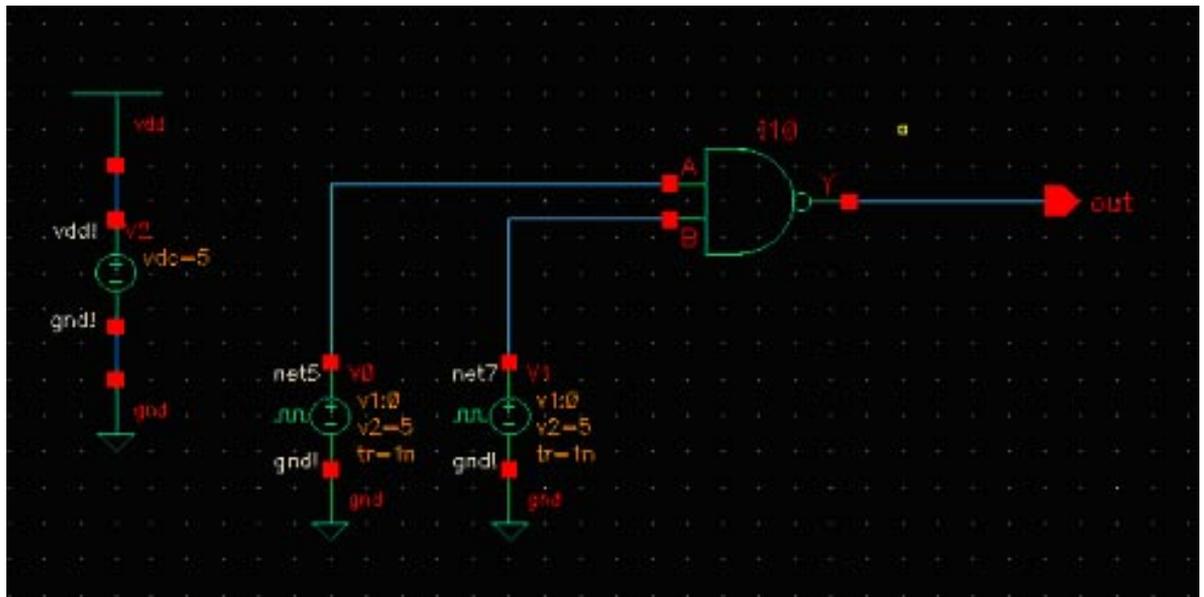


Figure 7.36: Test schematic for power measurements of a NAND gate

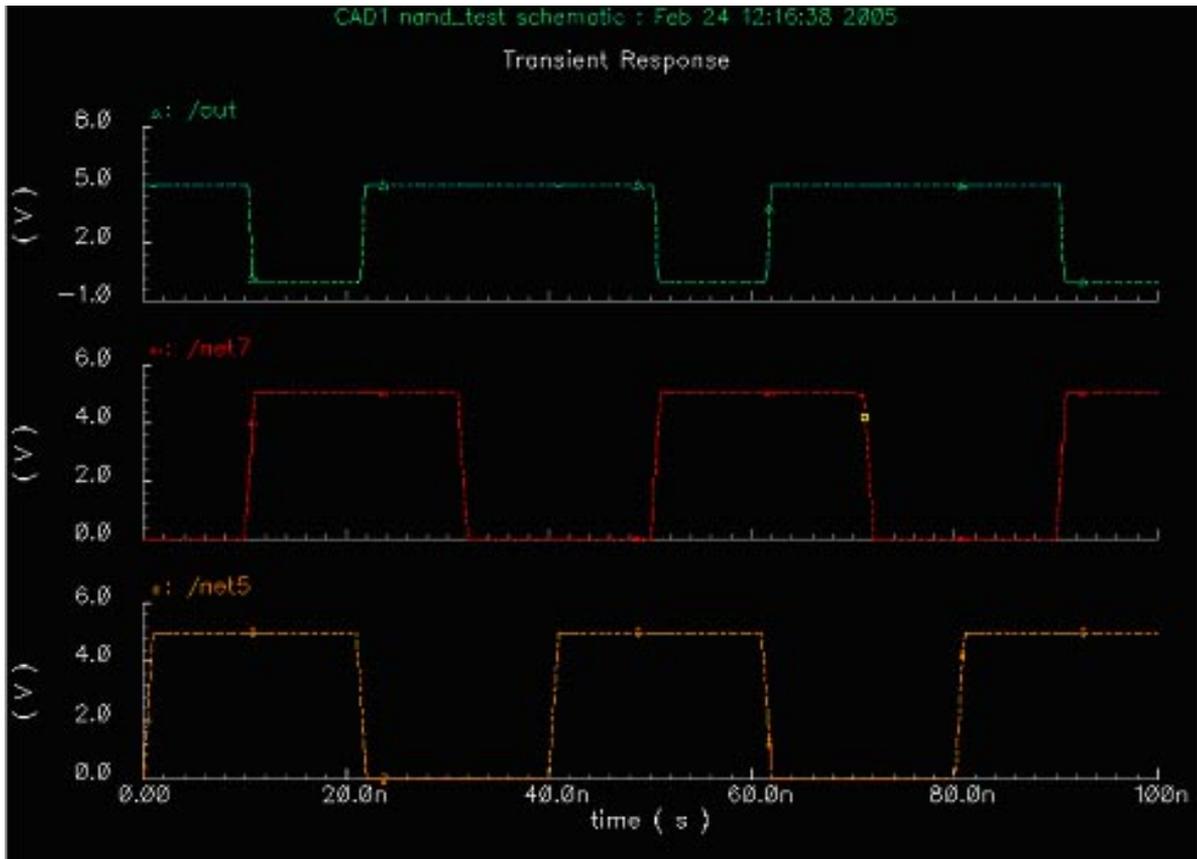


Figure 7.37: Analog simulation output from NAND gate simulation using *Spectre*

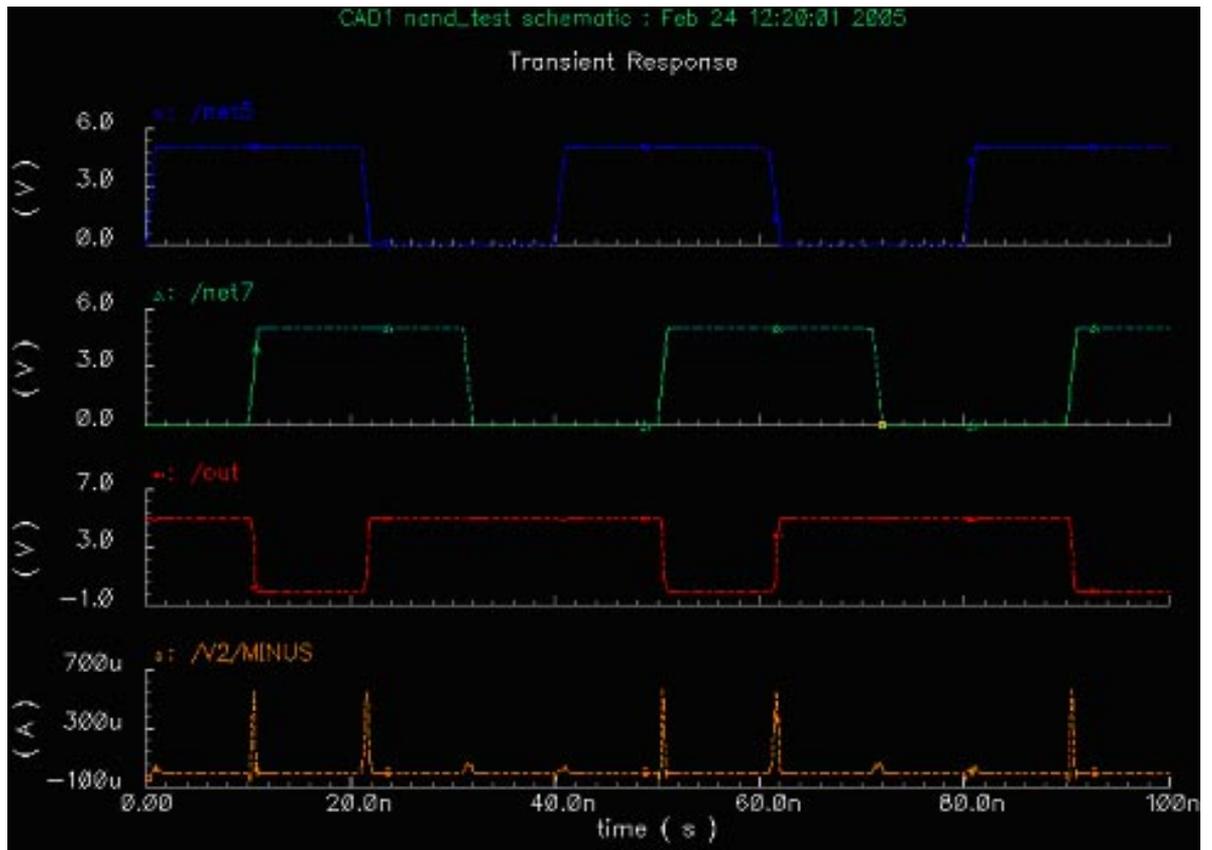
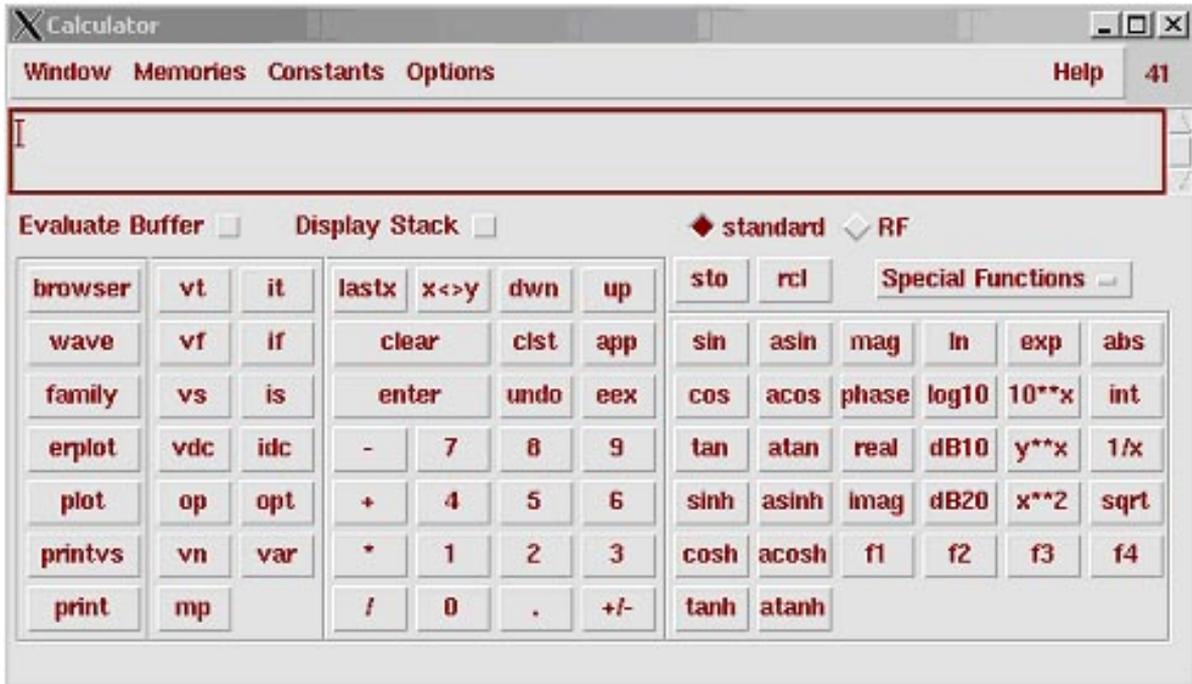


Figure 7.38: Waveform output with current plotted for the NAND simulation



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Figure 7.39: Dialog box for the *Spectre Analog Environment* calculator