Chapter 5

Virtuoso Layout Editor

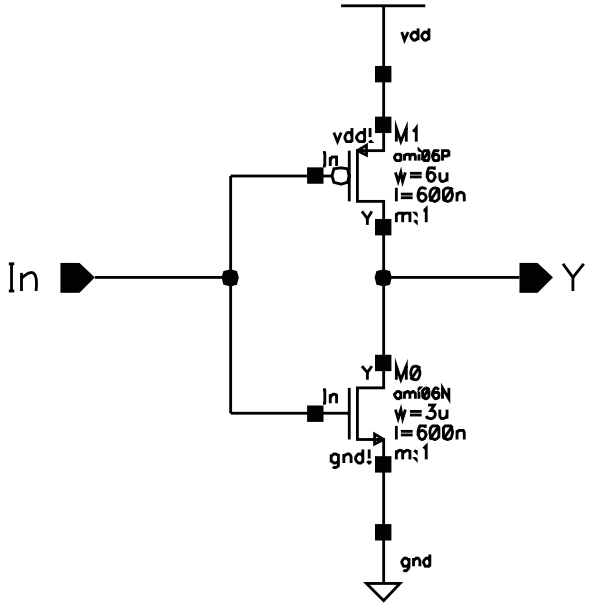

Figure 5.1: Inverter schematic

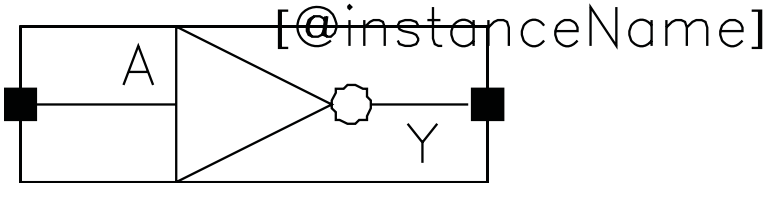

Figure 5.2: Inverter symbol

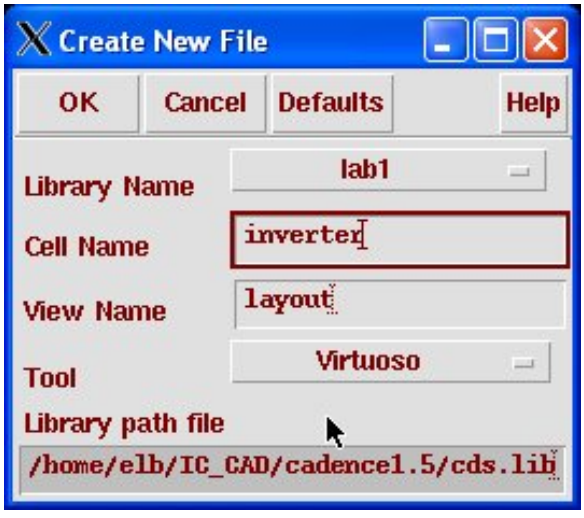

Figure 5.3: Dialog for creating a **Layout View** of the **inverter** cell

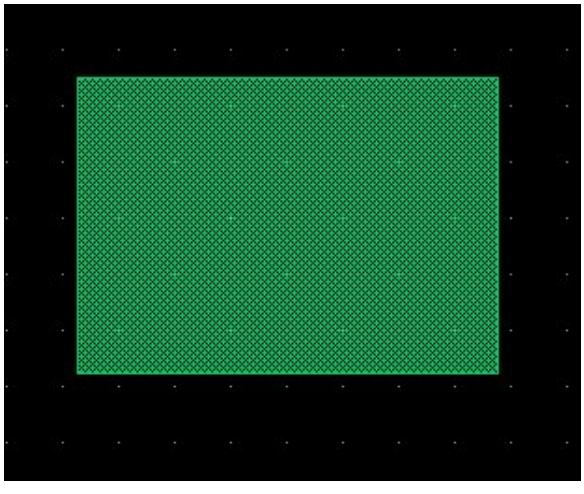

Figure 5.4: Initial **nactive** rectangle

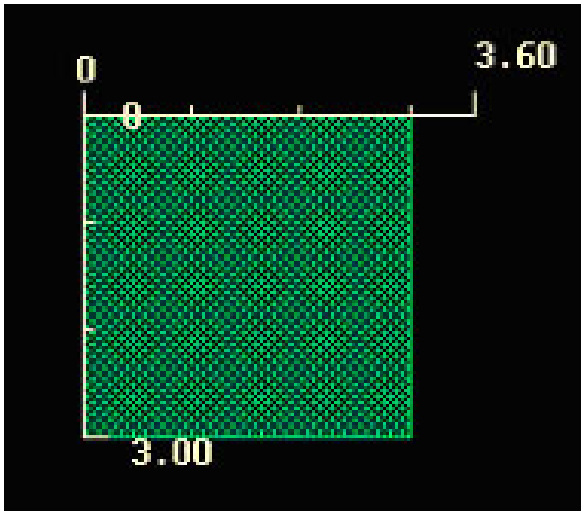

Figure 5.5: **nactive** rectangle with measurement rulers

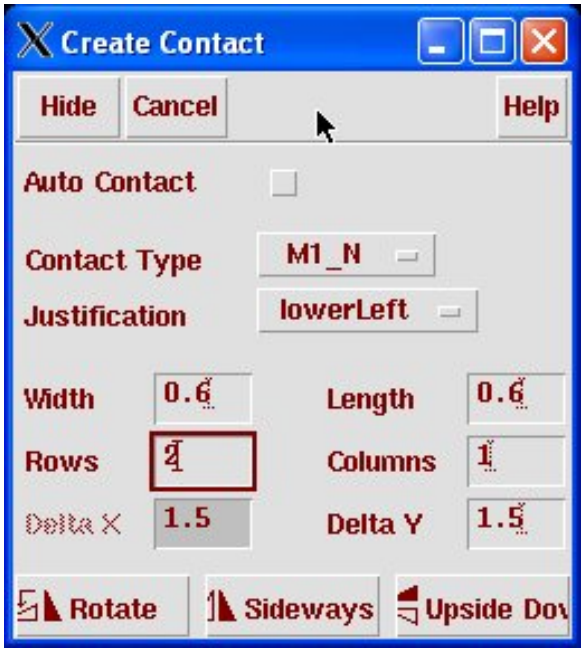

Figure 5.6: Create contact dialog box

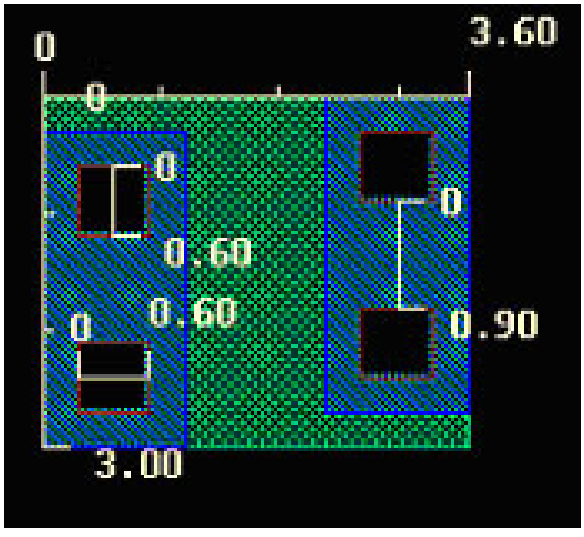

Figure 5.7: **nactive** showing source and drain connections

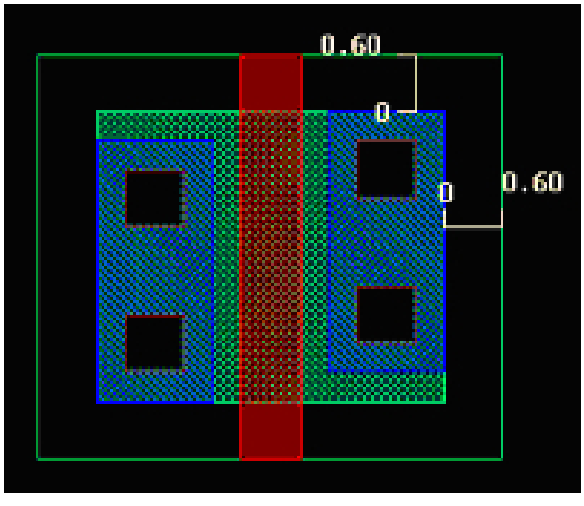

Figure 5.8: **Nmos** transistor 3μ wide and 0.6μ long

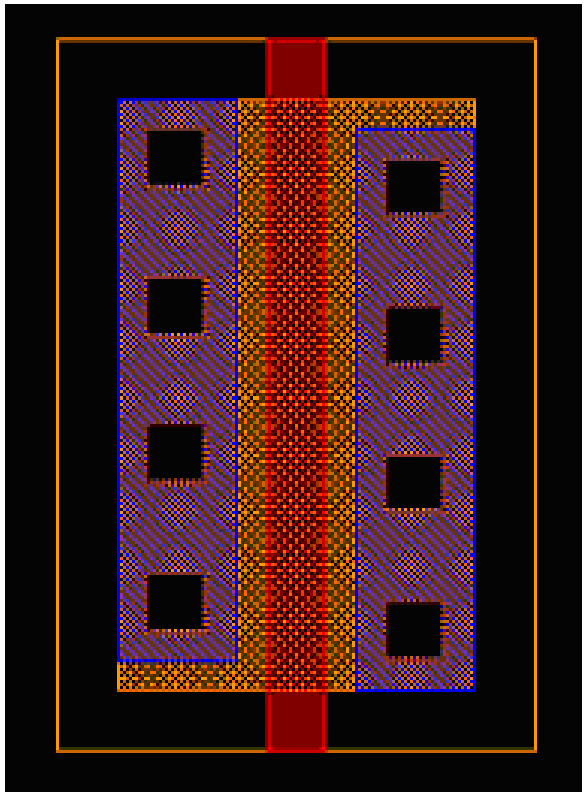

Figure 5.9: A **pmos** transistor 6μ wide and 0.6μ long

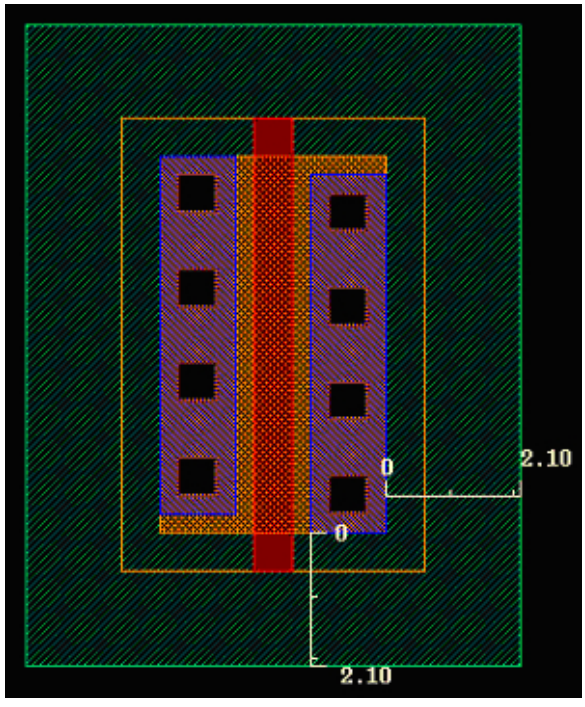

Figure 5.10: A **pmos** transistor inside of an **NWELL** region

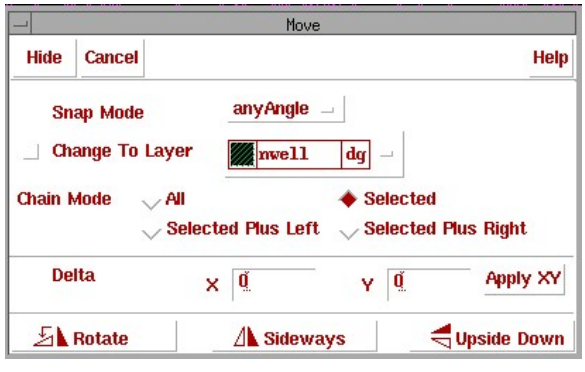

Figure 5.11: Extra features dialog box in move mode

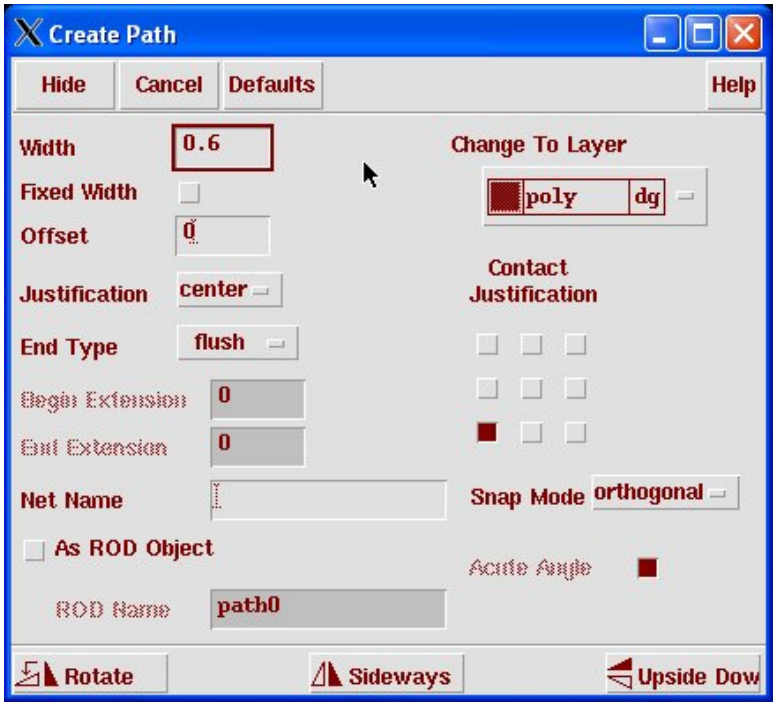

Figure 5.12: Dialog box for the **path** command

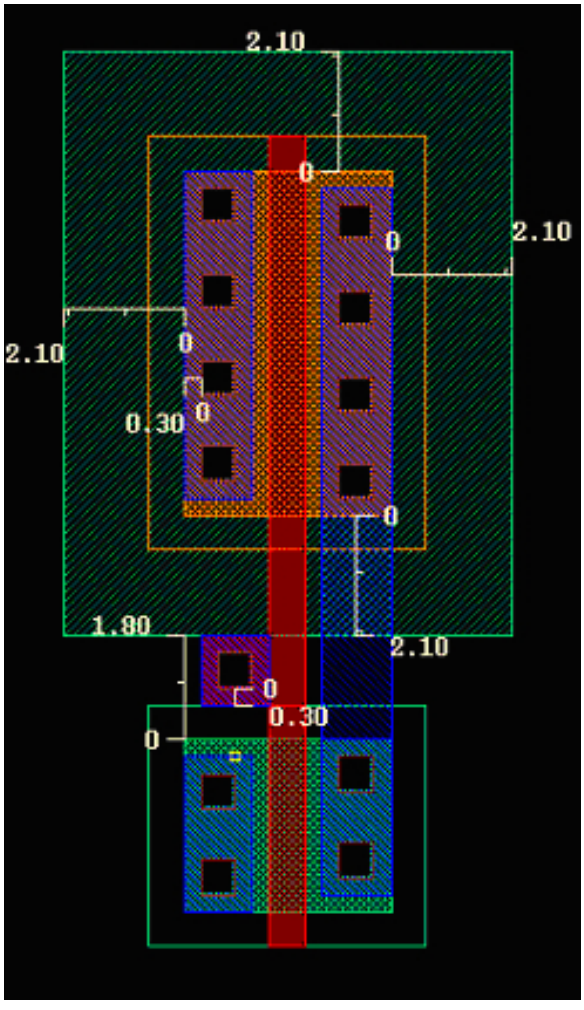

Figure 5.13: Inverter layout with input and output connections made

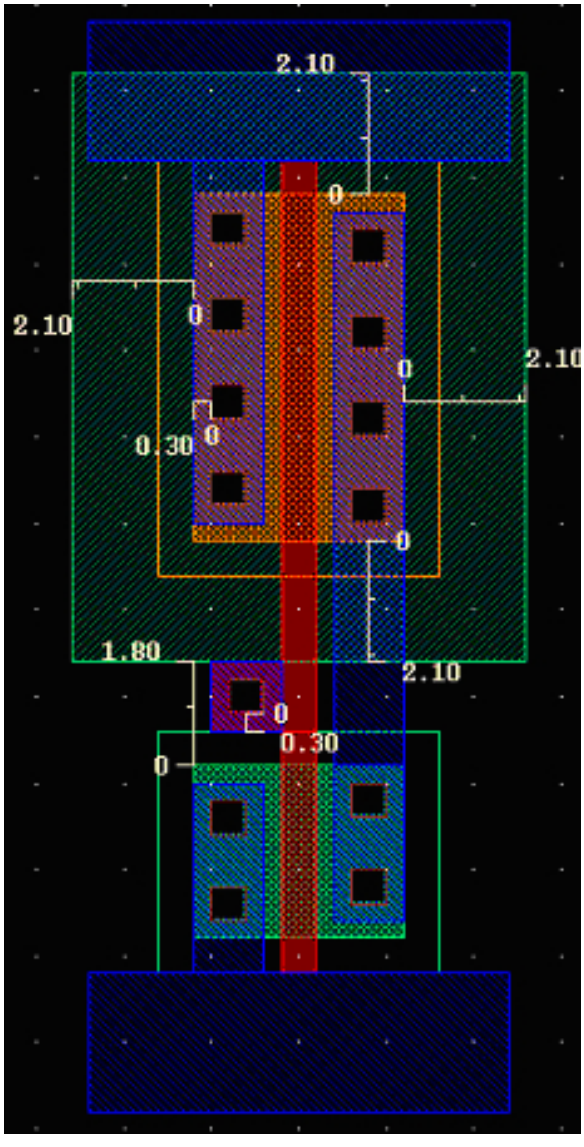

Figure 5.14: Inverter layout with power supply connections

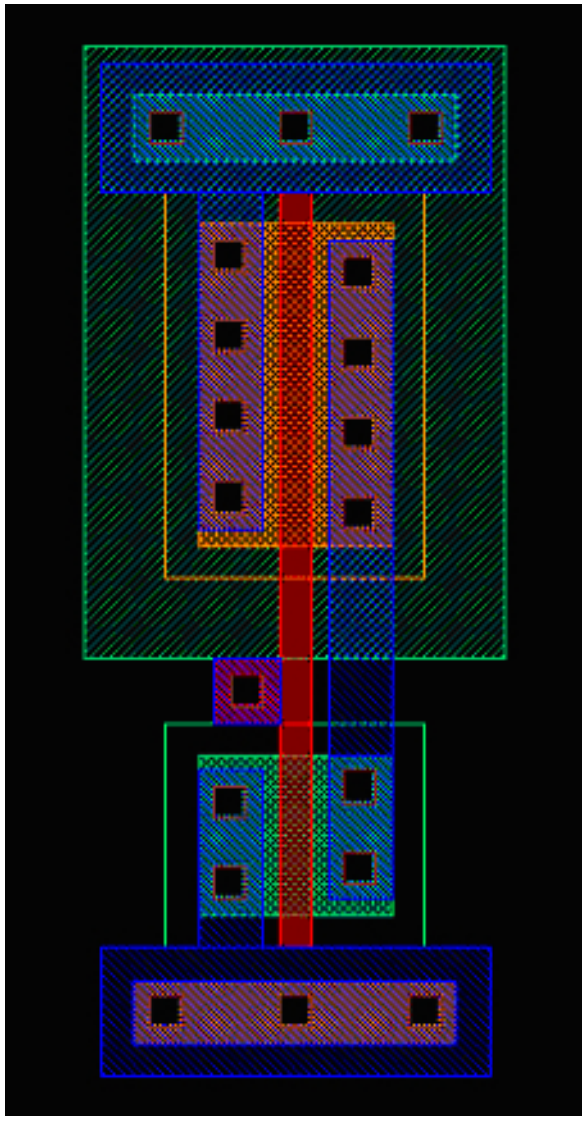

Figure 5.15: Inverter layout with well and substrate connections

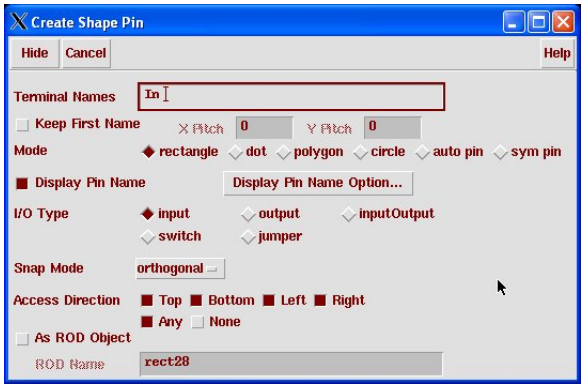

Figure 5.16: Shape pin dialog box

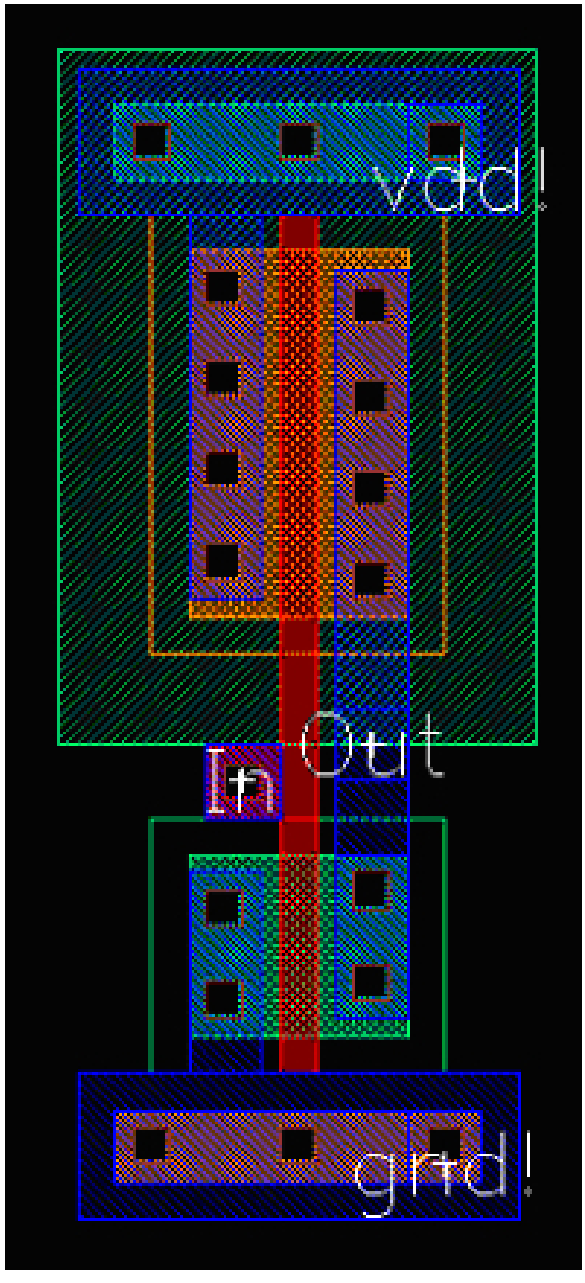

Figure 5.17: Final inverter layout

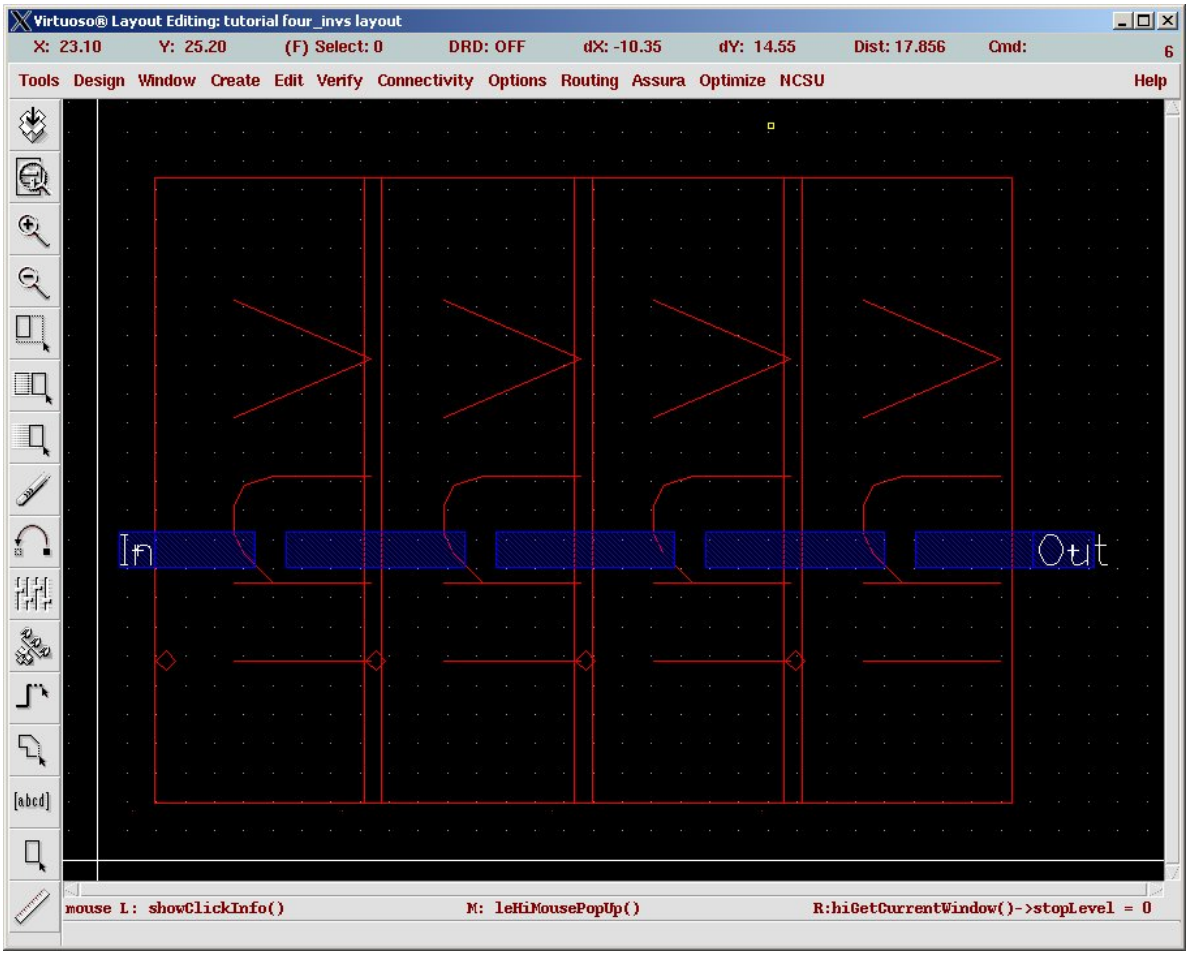

Figure 5.18: Layout with four inverter instances

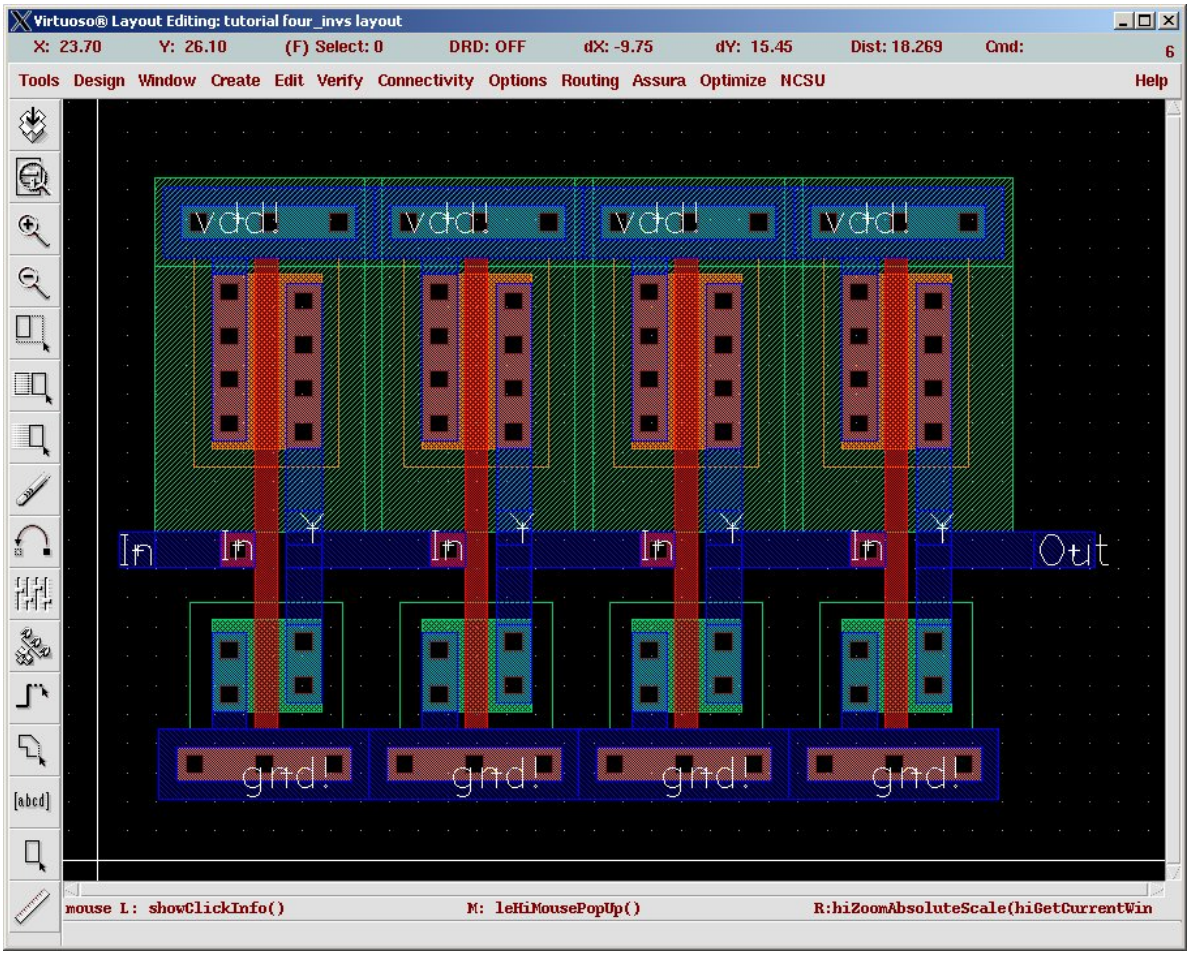

Figure 5.19: Layout with four inverter instances expanded to see all levels of layout

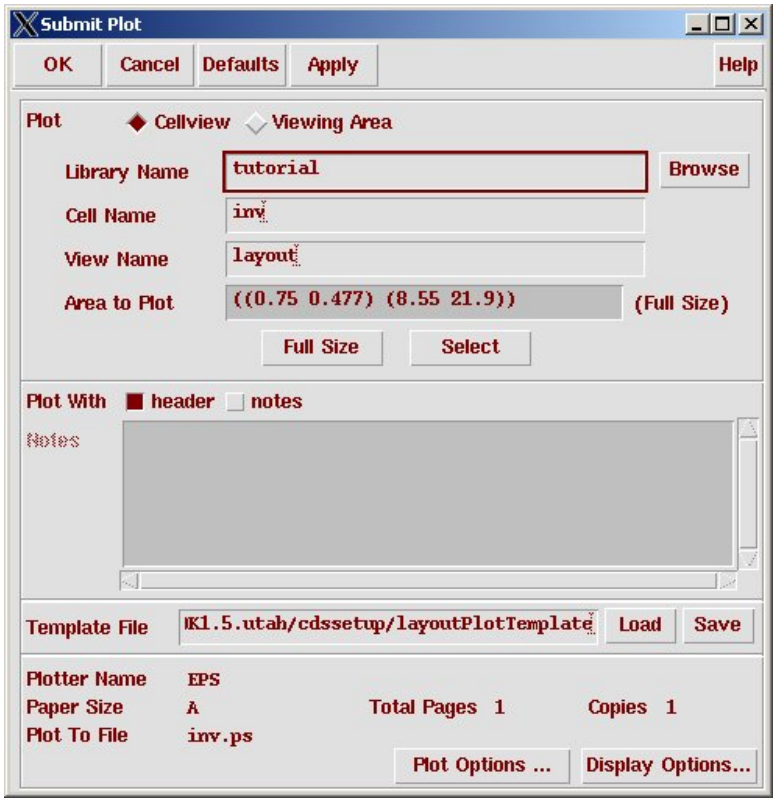

Figure 5.20: Submit Plot dialog box

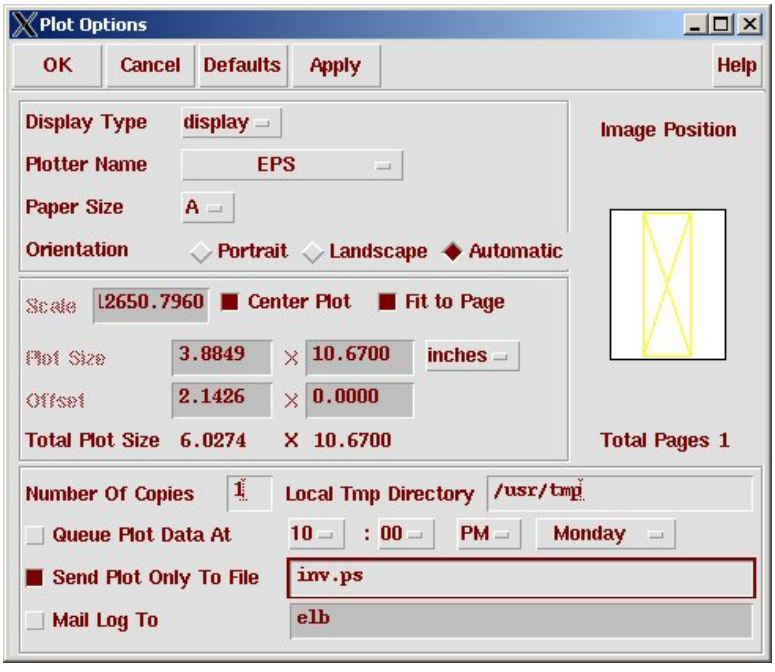

Figure 5.21: Plot Options dialog box

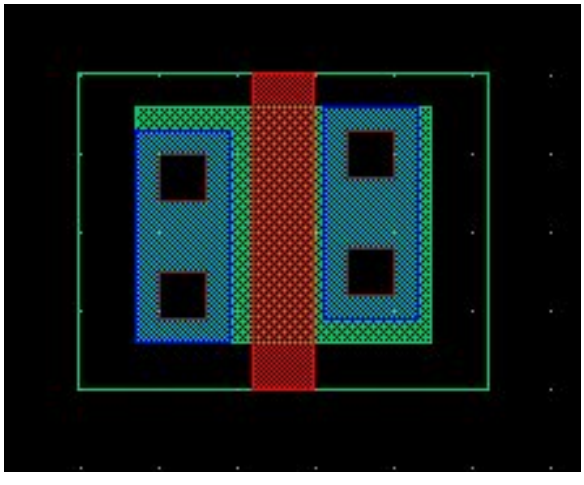

Figure 5.22: Nmos transistor layout (with *DRC* errors)

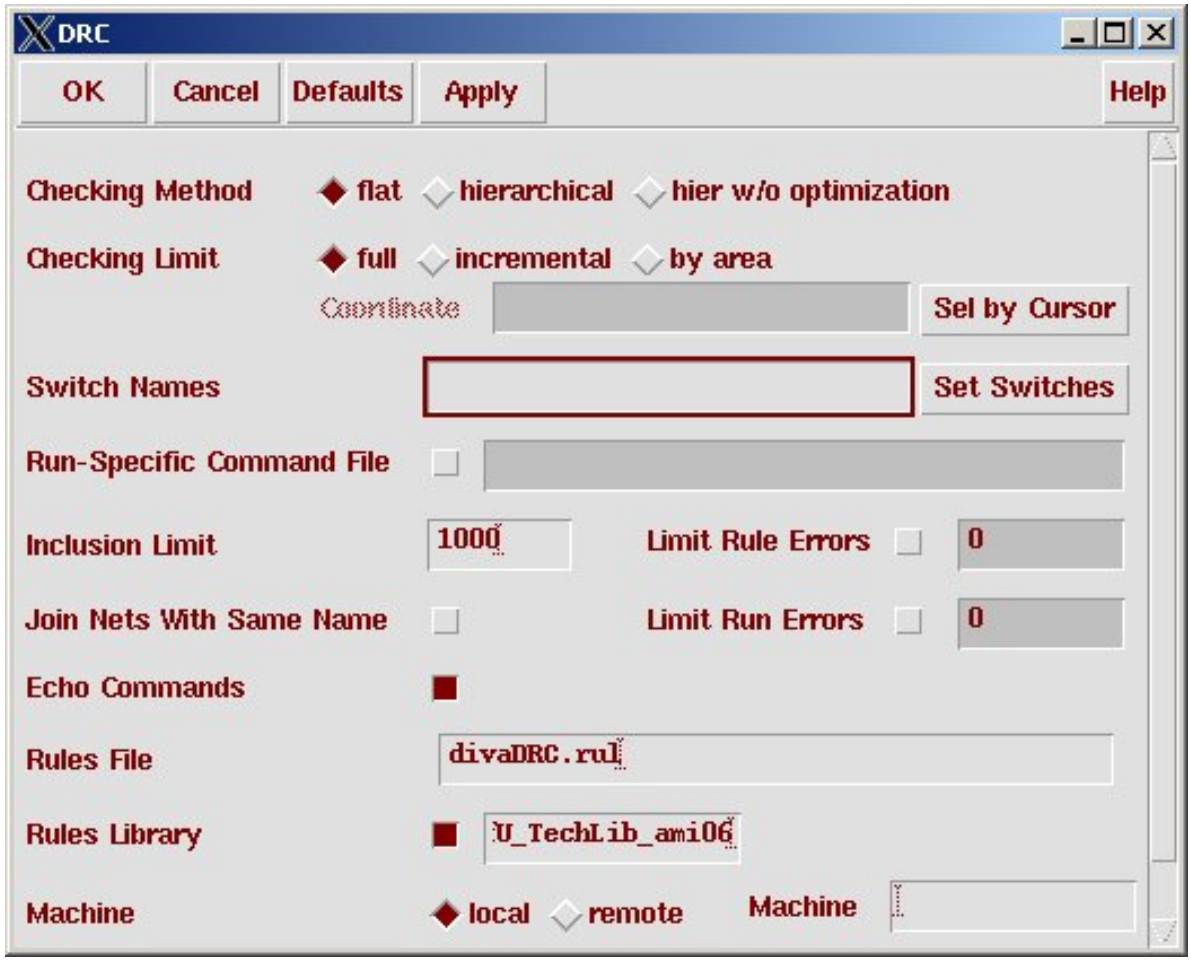

Figure 5.23: *DIVA DRC* control window

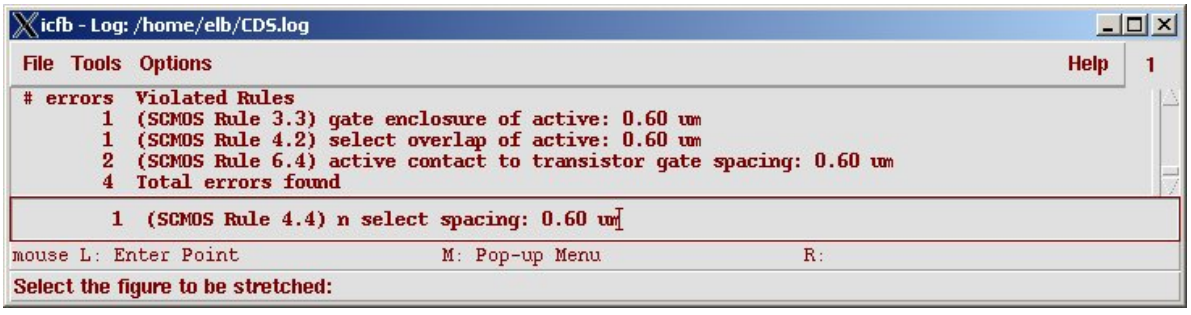

Figure 5.24: Results from the *DRC* in the **CIW** window

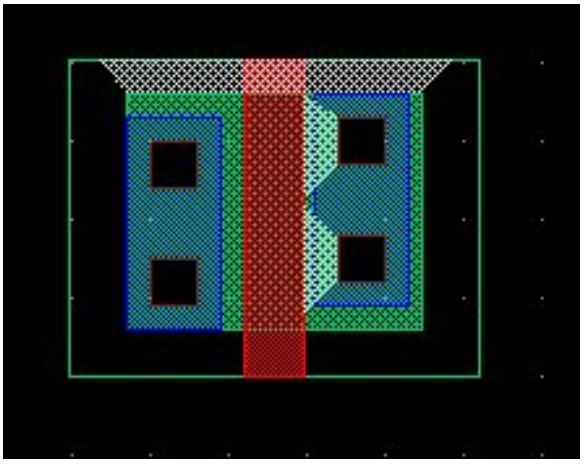

Figure 5.25: **Nmos** transistor layout (with *DRC* errors flagged)

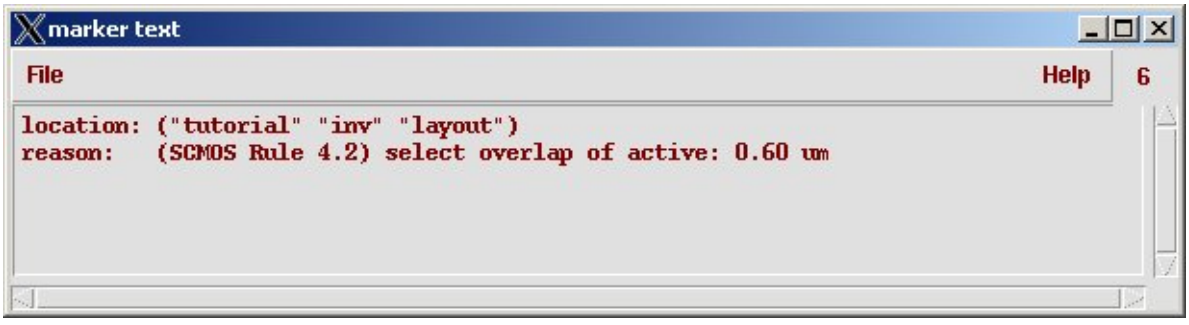

Figure 5.26: Explanation of *DRC* violation

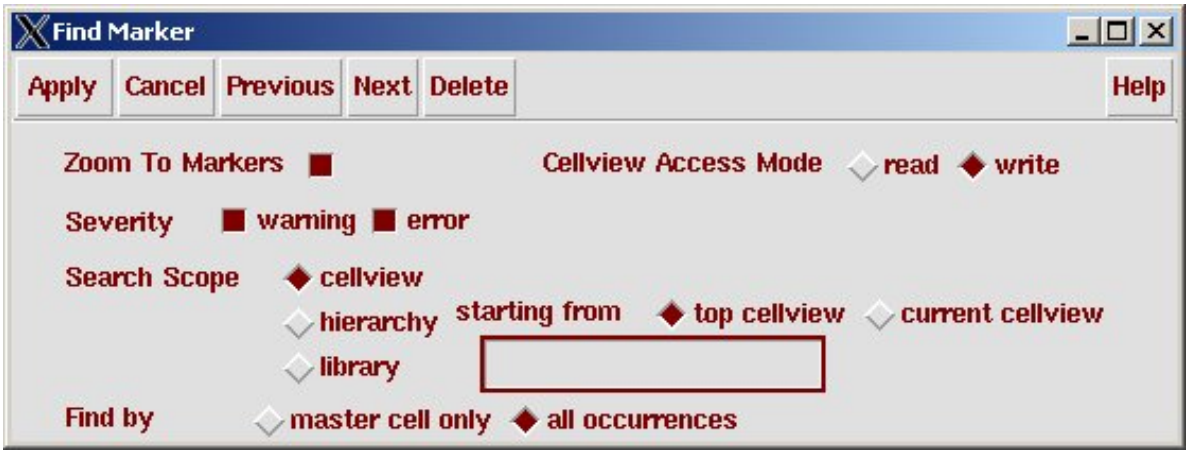

Figure 5.27: Finding all *DRC* violations

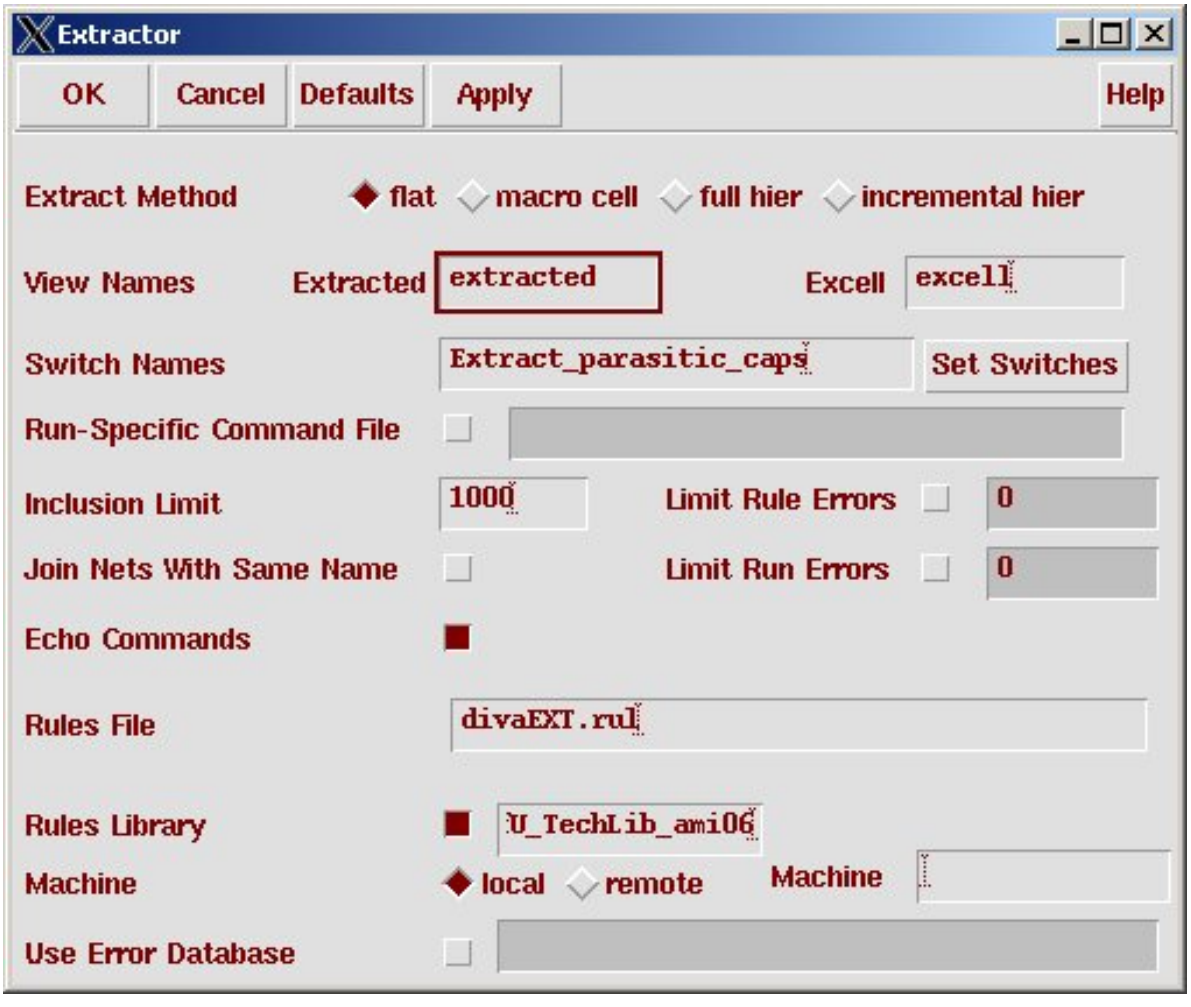

Figure 5.28: *DIVA* extraction control window

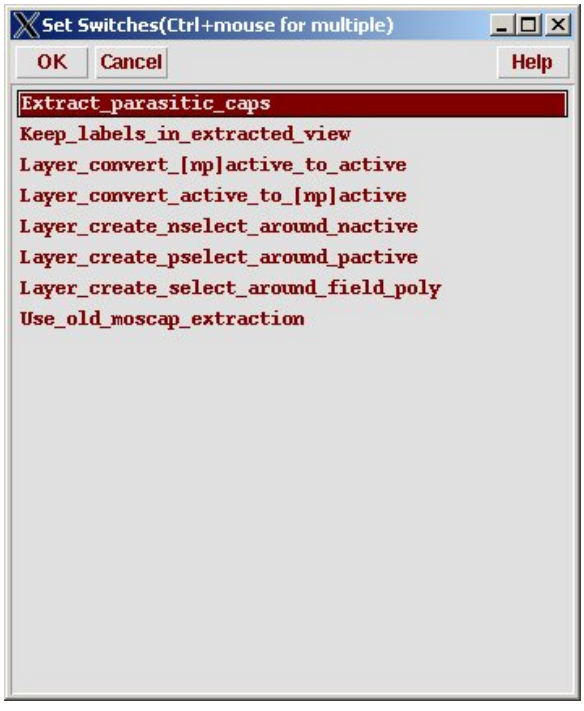

Figure 5.29: *DIVA* extraction special switches

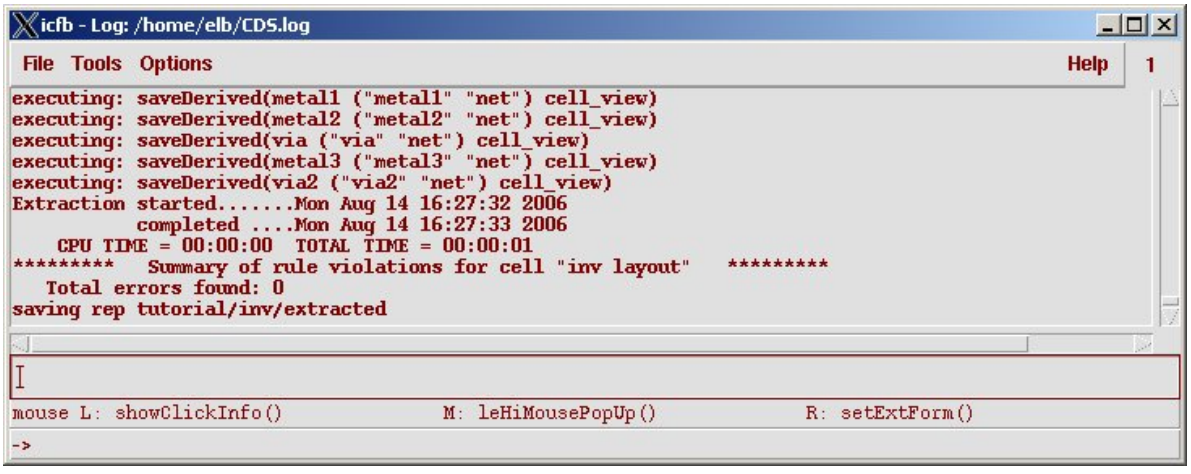

Figure 5.30: *DIVA* extraction result in the CIW

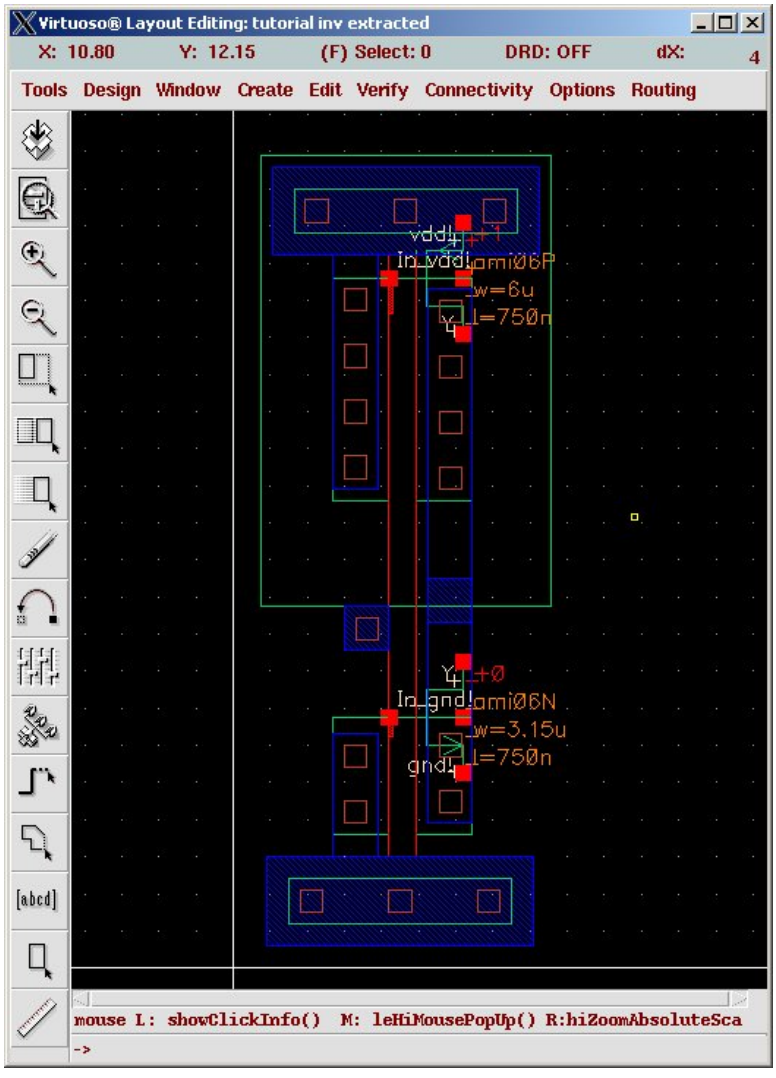

Figure 5.31: Extracted view of the inverter

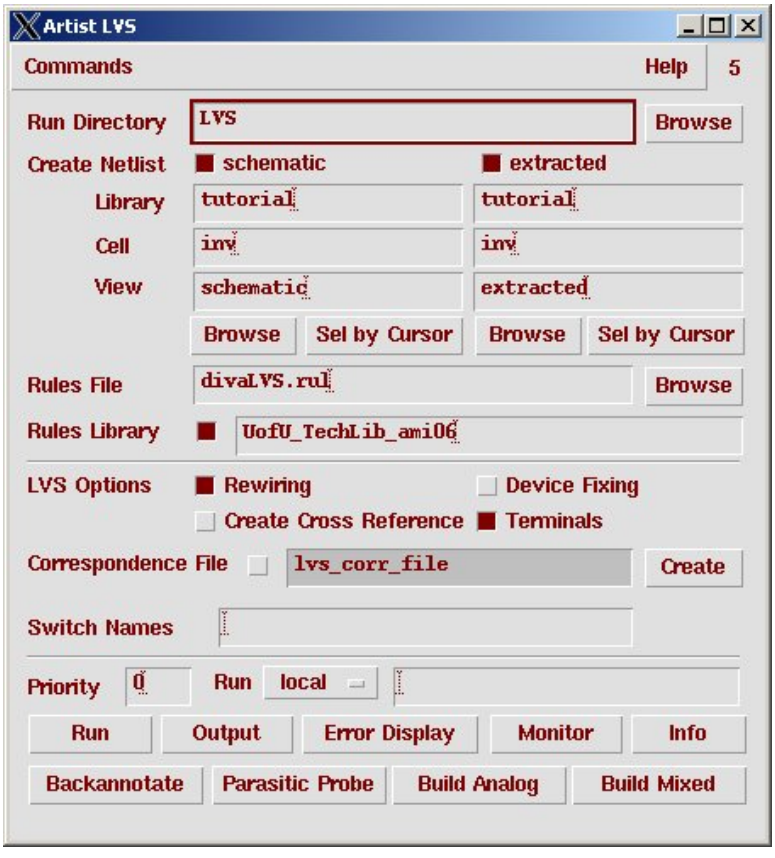

Figure 5.32: *DIVA LVS* control window

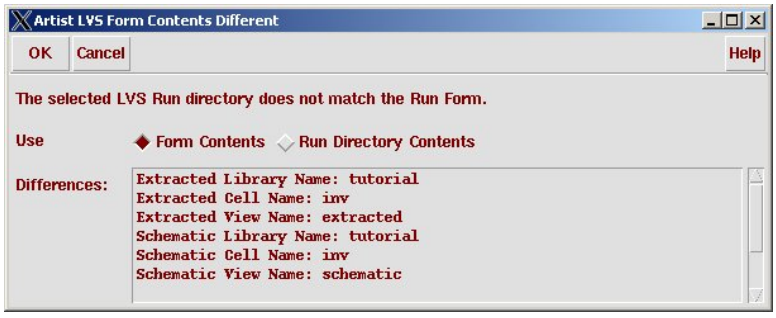

Figure 5.33: *DIVA LVS* Control Form

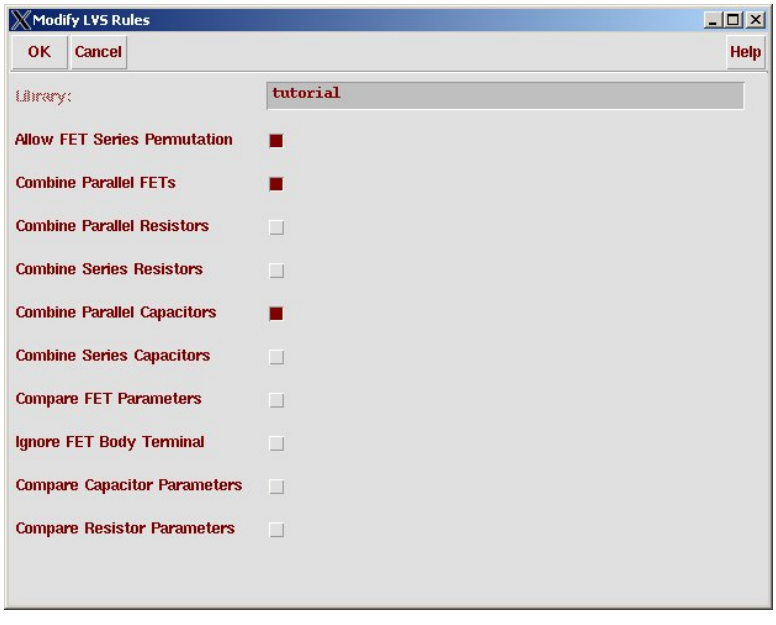

Figure 5.34: NCSU form to modify *LVS* rules

Figure 5.35: *DIVA LVS* completion indication

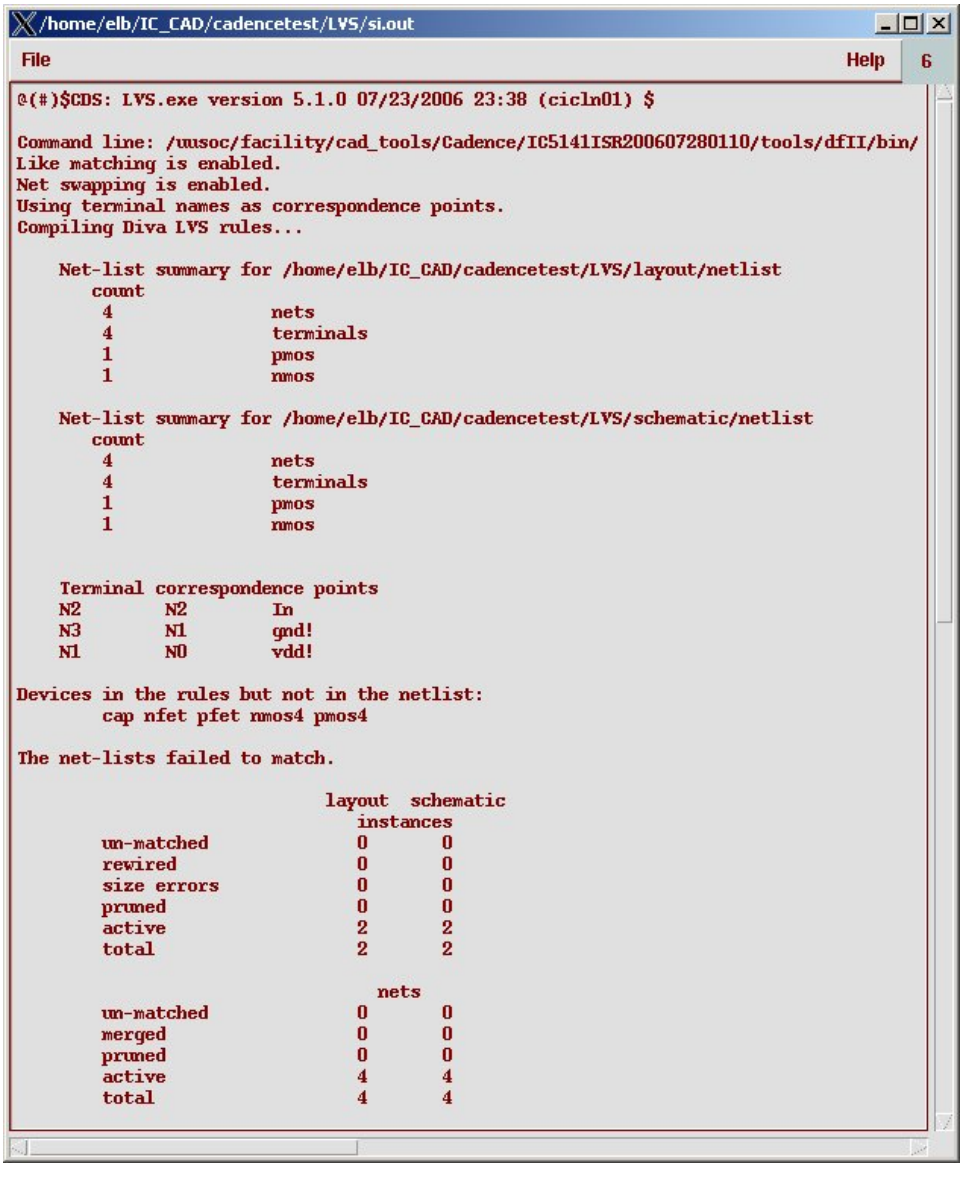

Figure 5.36: *DIVA LVS* output

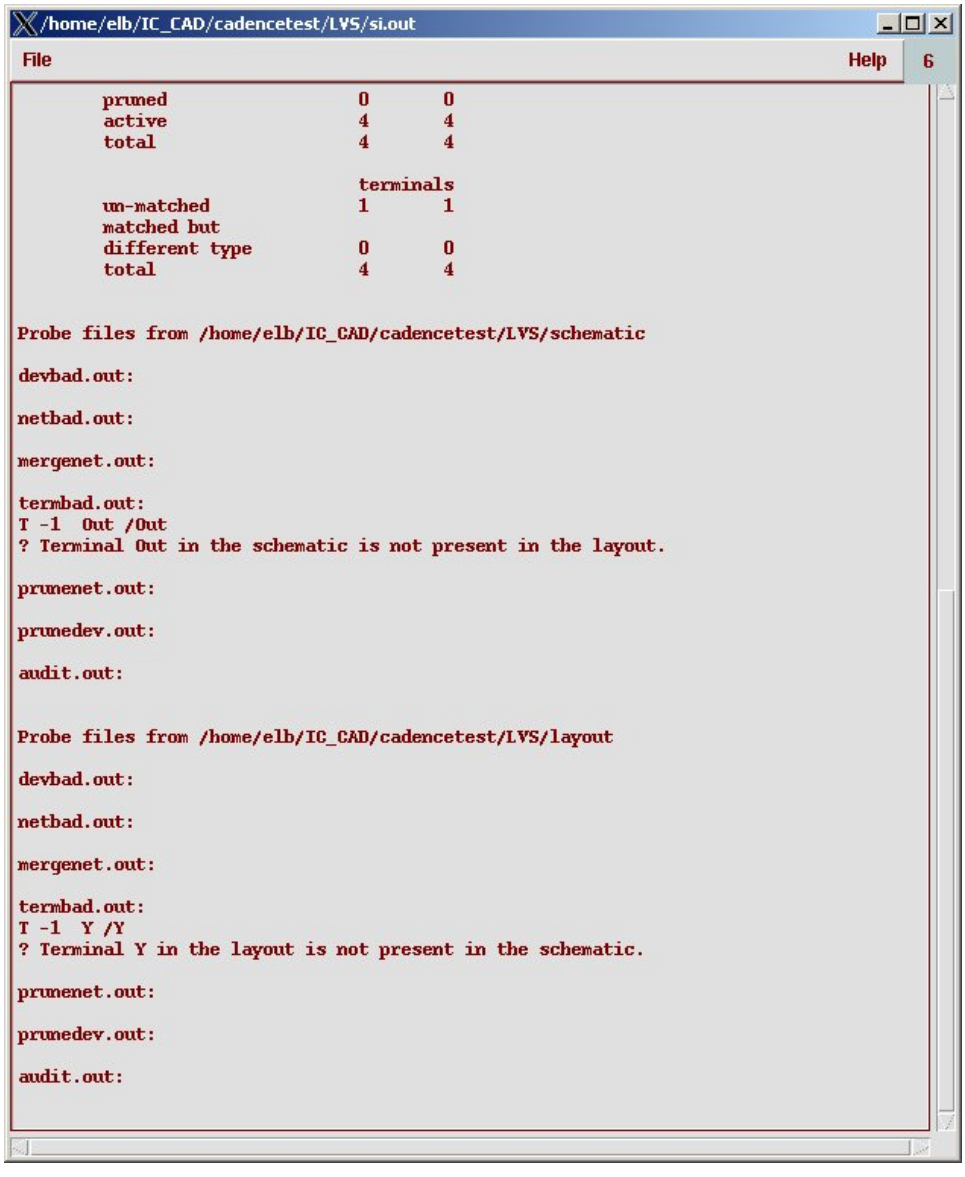

Figure 5.37: *DIVA LVS* output (scrolled)

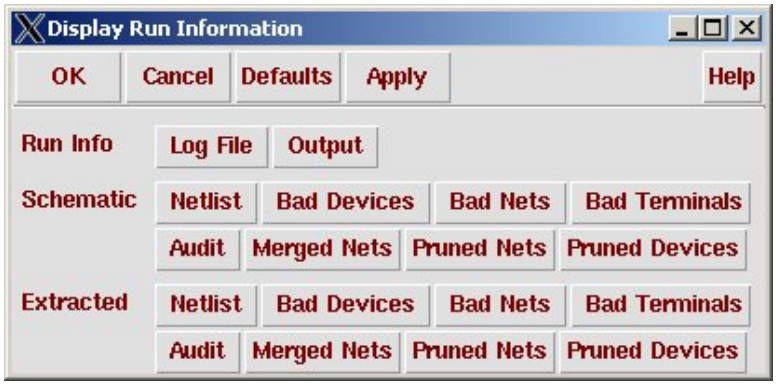

Figure 5.38: *DIVA LVS* Run Information window