

Chapter **5**

Virtuoso Layout Editor

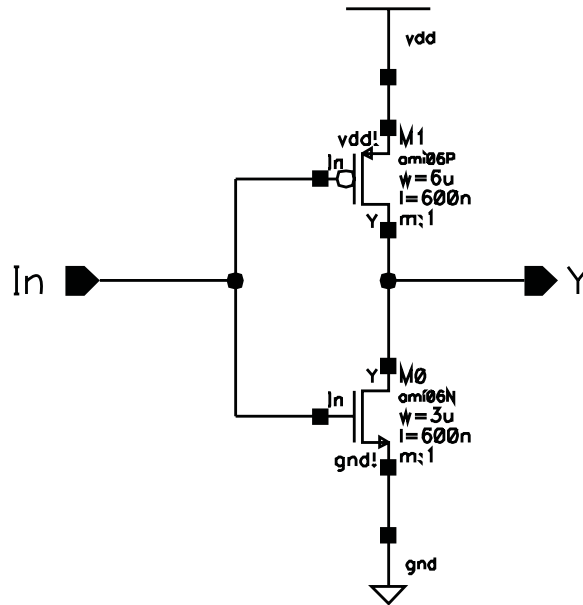


Figure 5.1: Inverter schematic

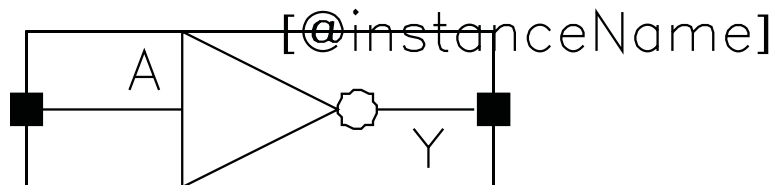
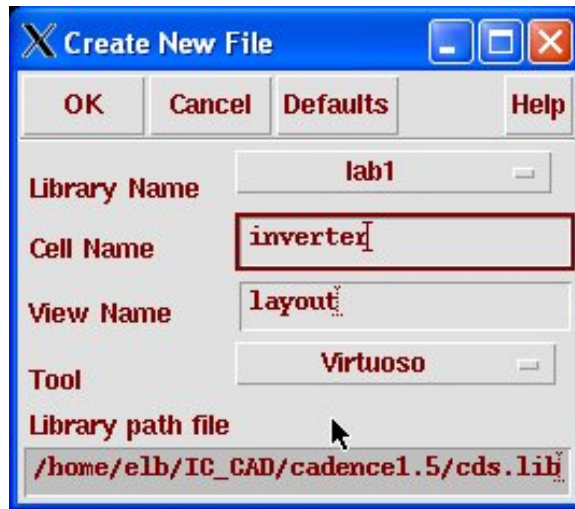


Figure 5.2: Inverter symbol



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Figure 5.3: Dialog for creating a Layout View of the inverter cell

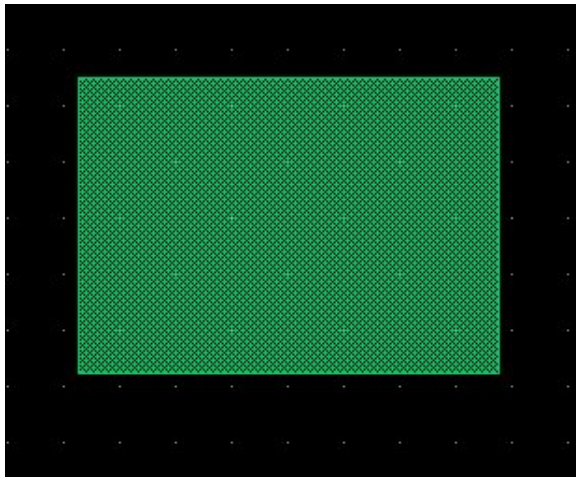


Figure 5.4: Initial nactive rectangle

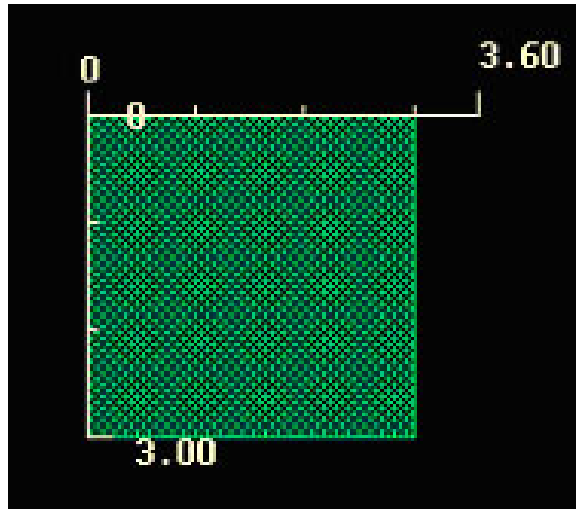
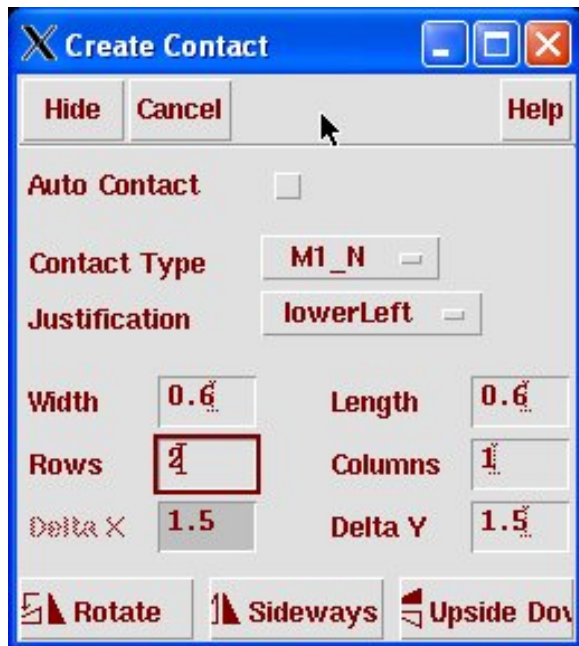


Figure 5.5: nactive rectangle with measurement rulers



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Figure 5.6: Create contact dialog box

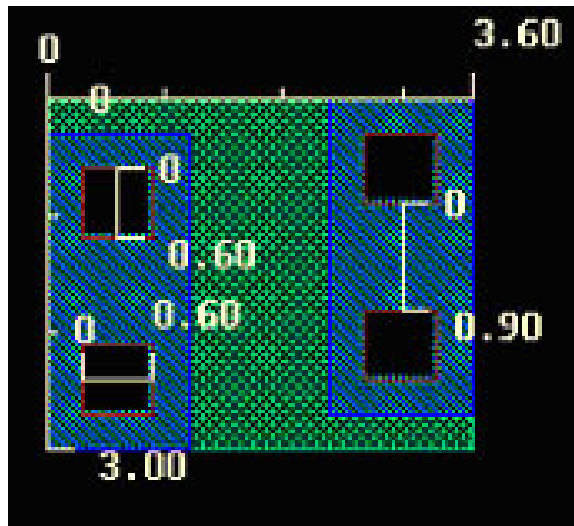


Figure 5.7: nactive showing source and drain connections

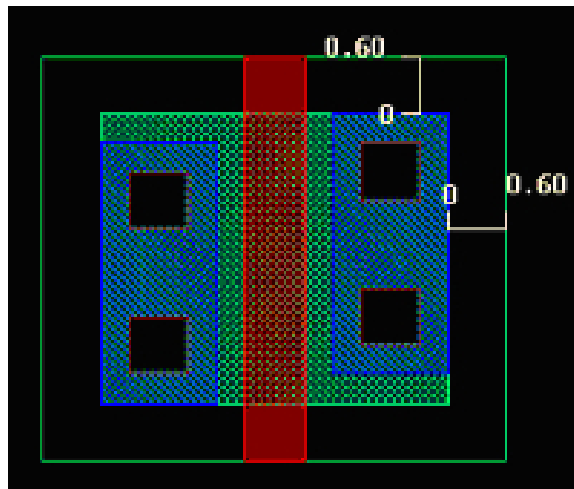


Figure 5.8: Nmos transistor 3μ wide and 0.6μ long

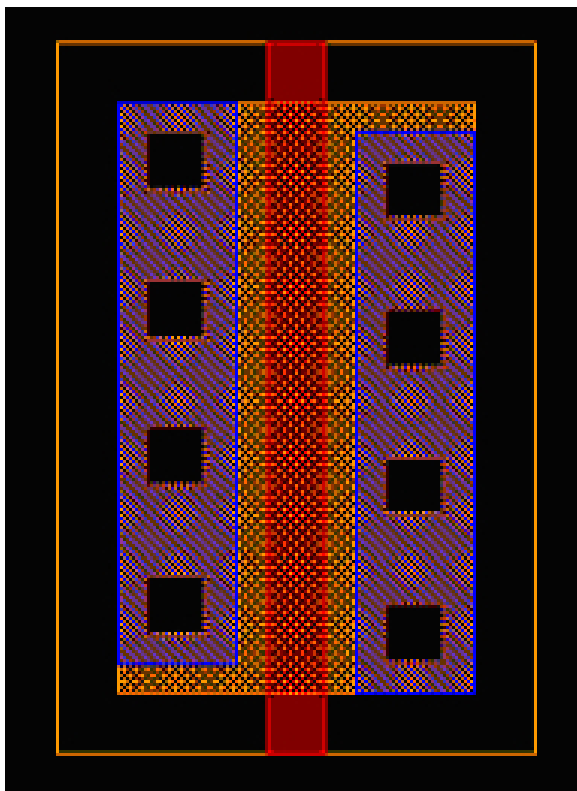


Figure 5.9: A pmos transistor 6μ wide and 0.6μ long

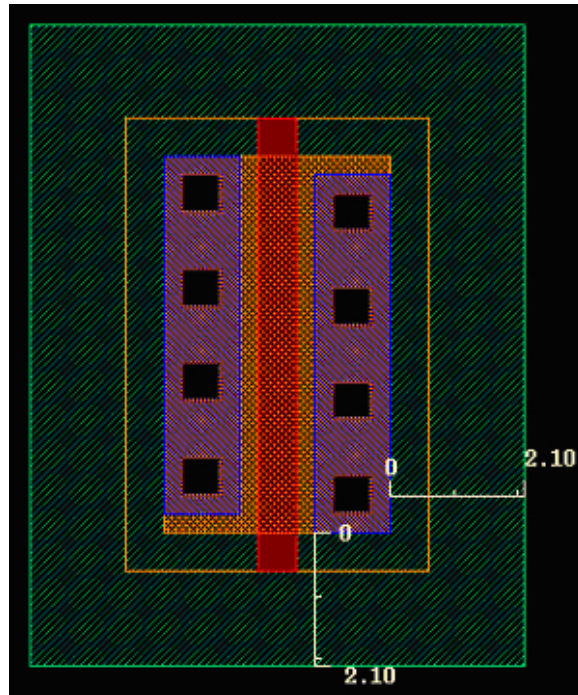
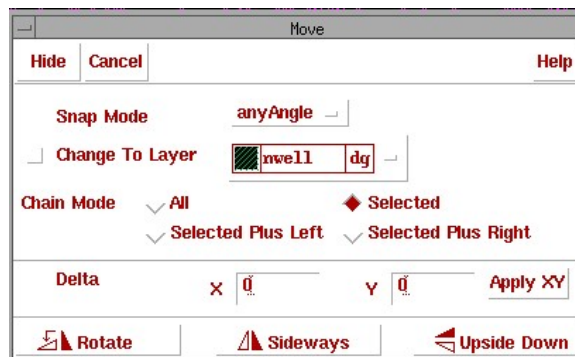
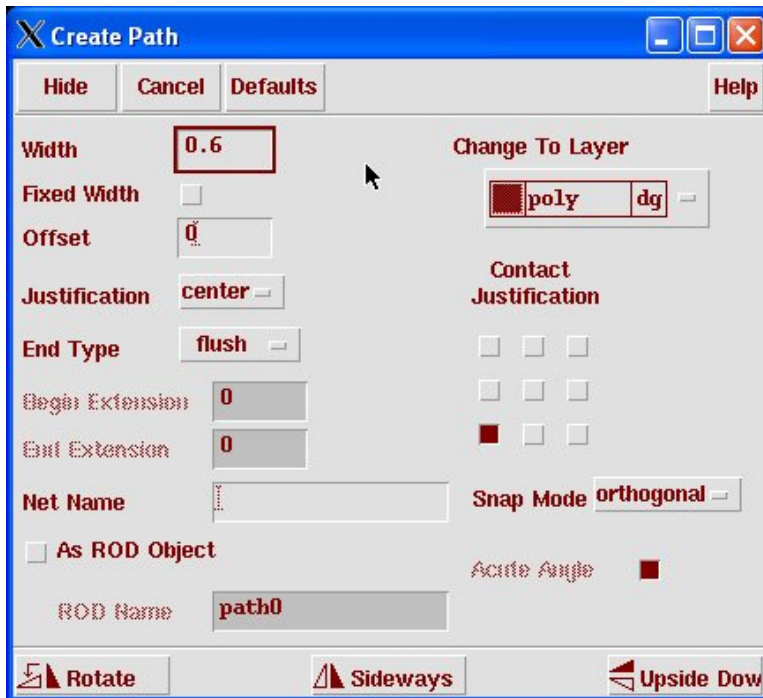


Figure 5.10: A pmos transistor inside of an NWELL region



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Figure 5.11: Extra features dialog box in move mode



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Figure 5.12: Dialog box for the path command

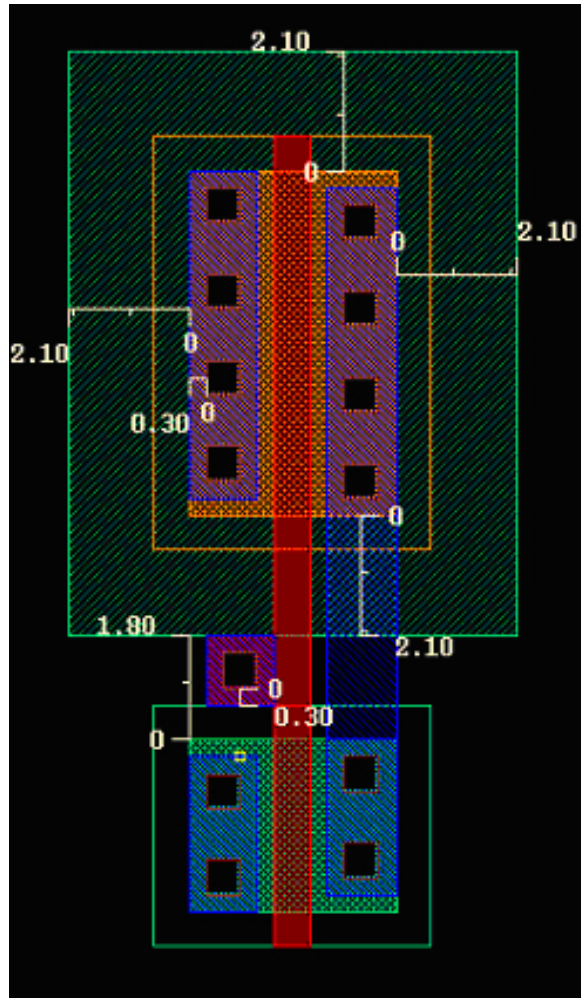


Figure 5.13: Inverter layout with input and output connections made

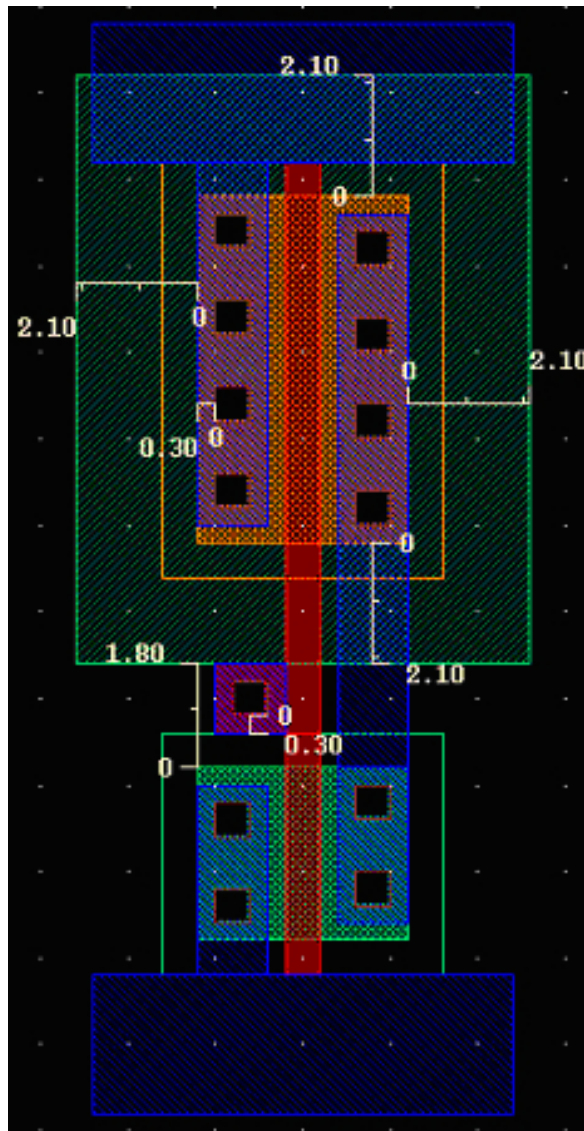


Figure 5.14: Inverter layout with power supply connections

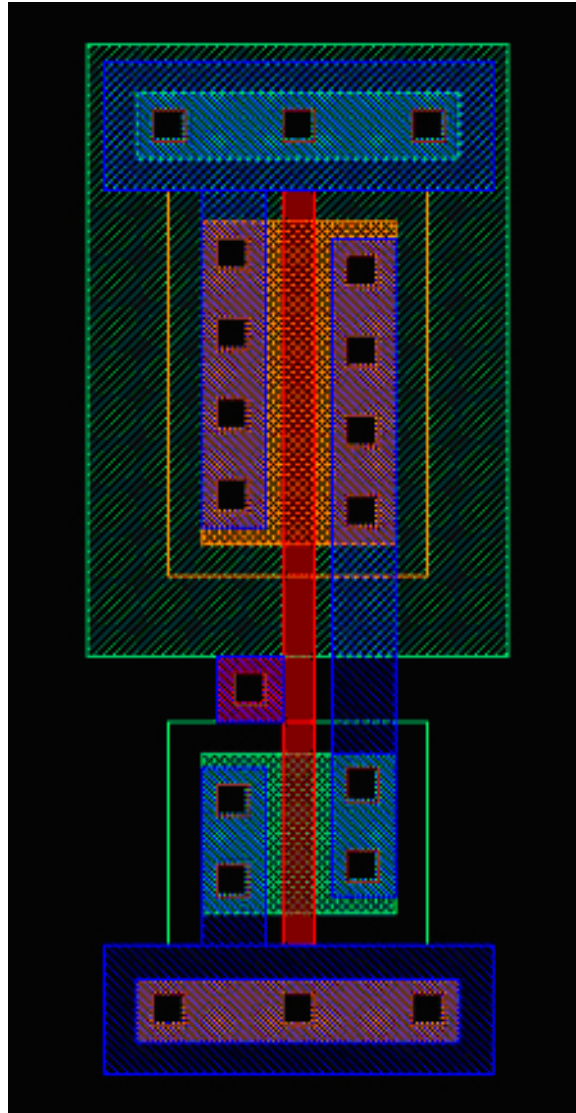
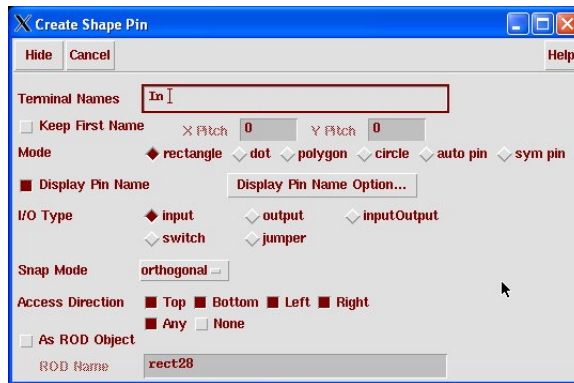
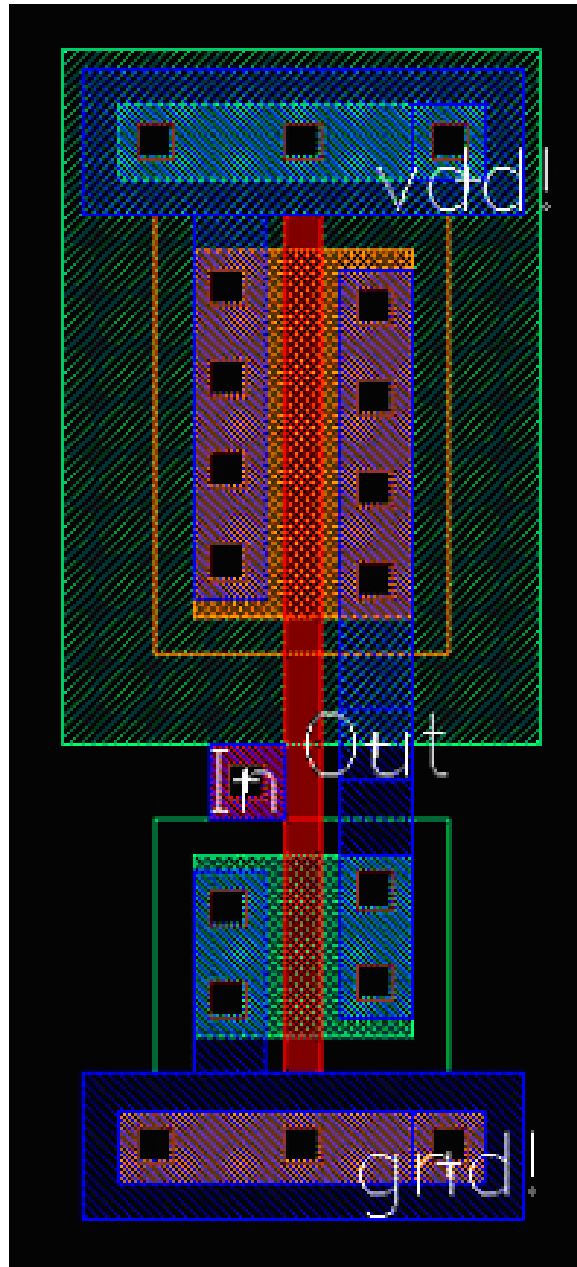


Figure 5.15: Inverter layout with well and substrate connections



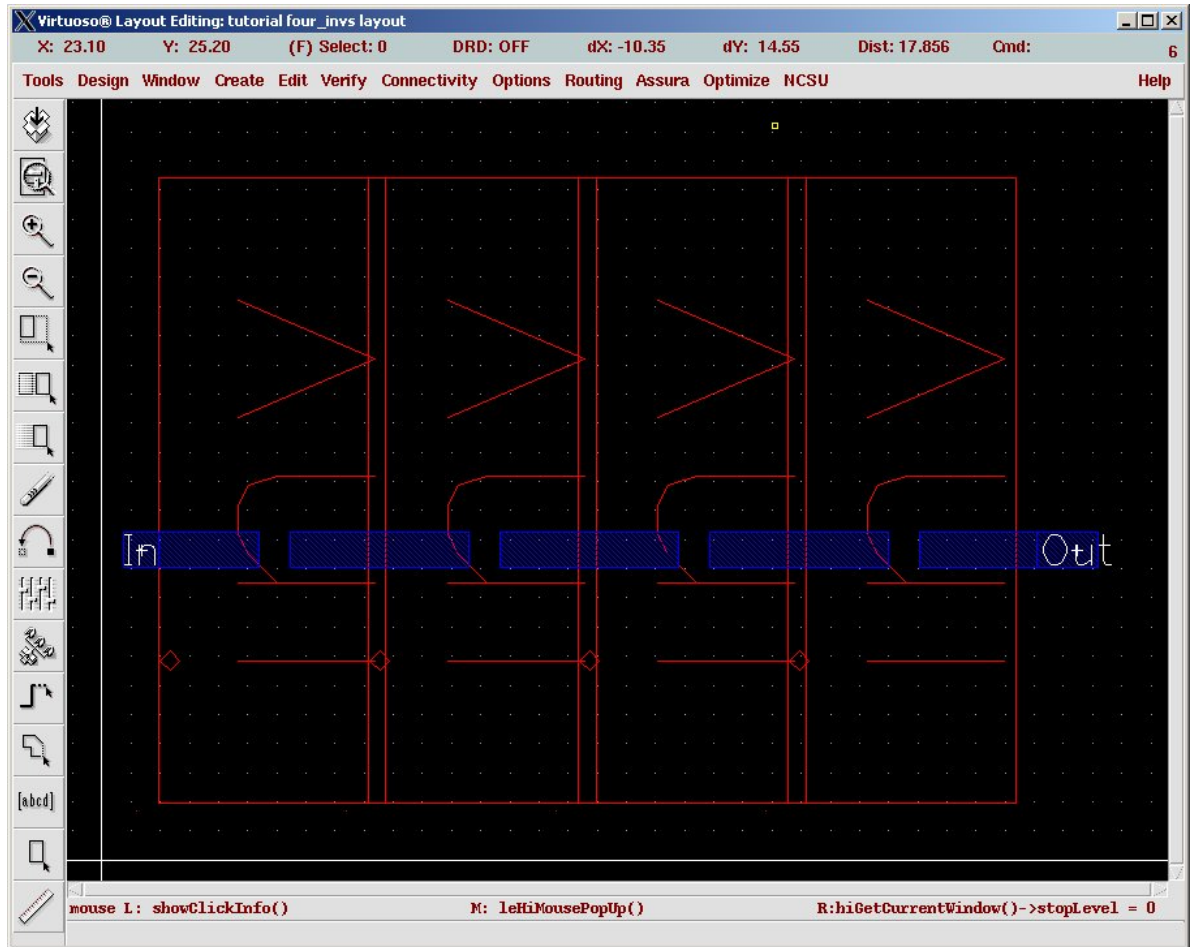
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Figure 5.16: Shape pin dialog box



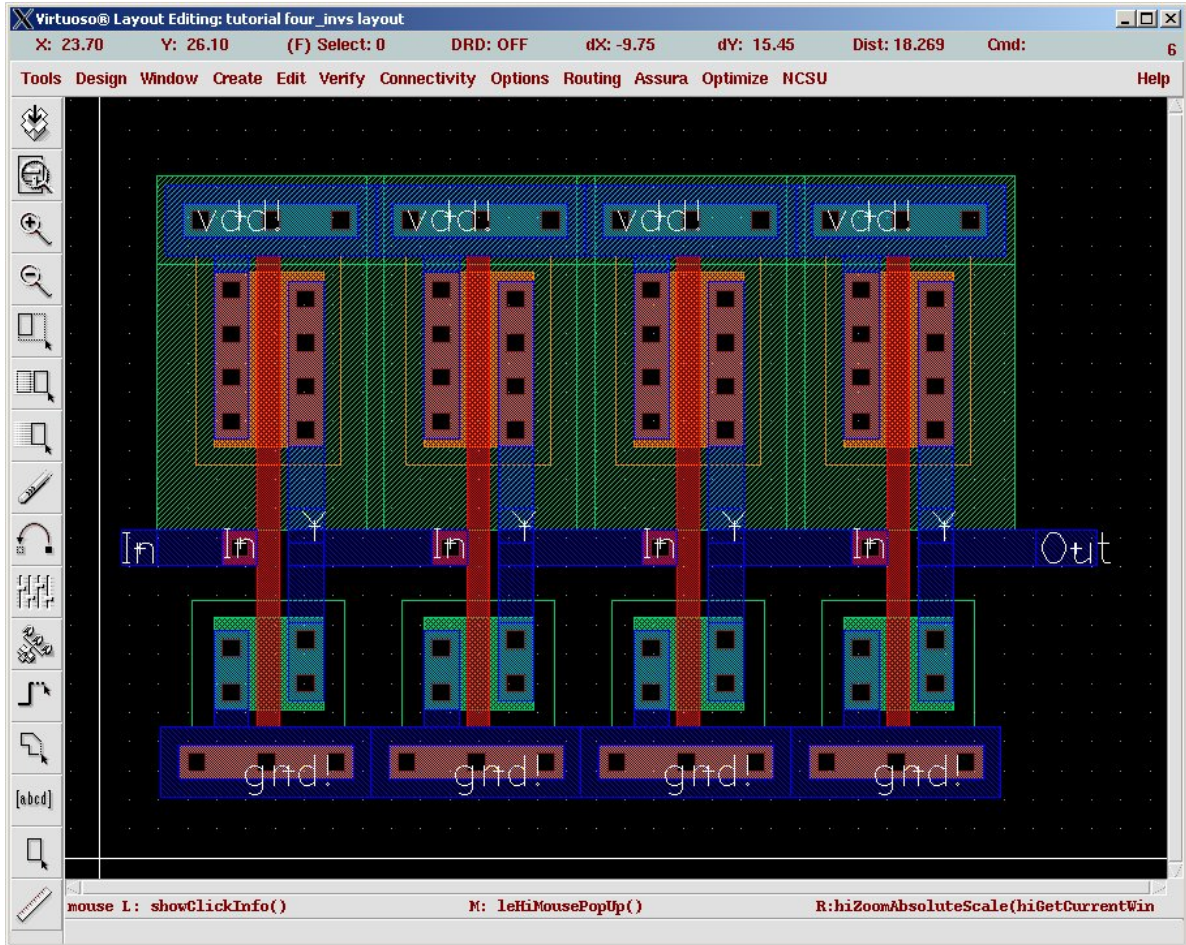
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Figure 5.17: Final inverter layout



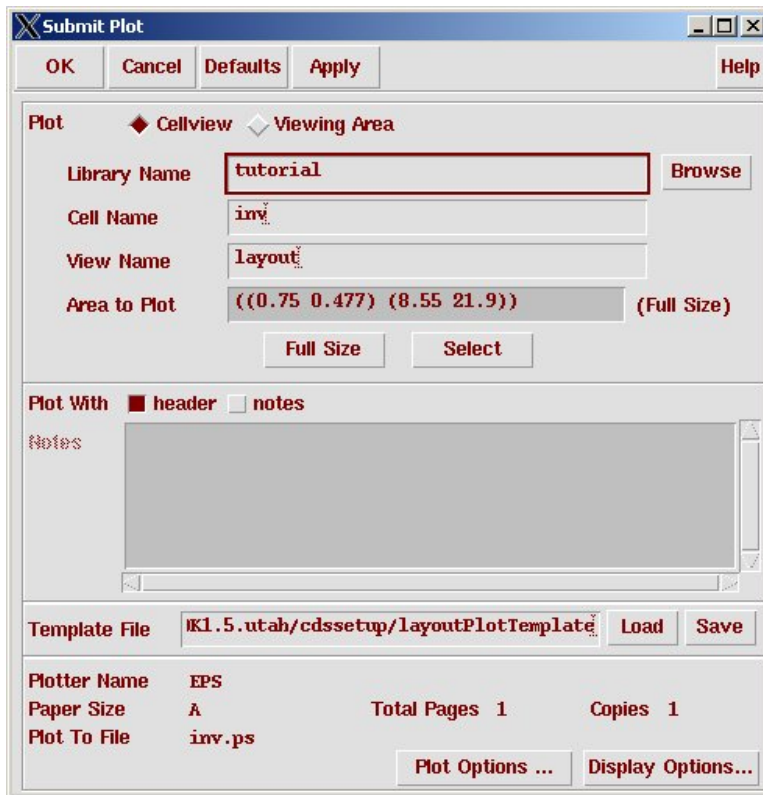
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Figure 5.18: Layout with four inverter instances



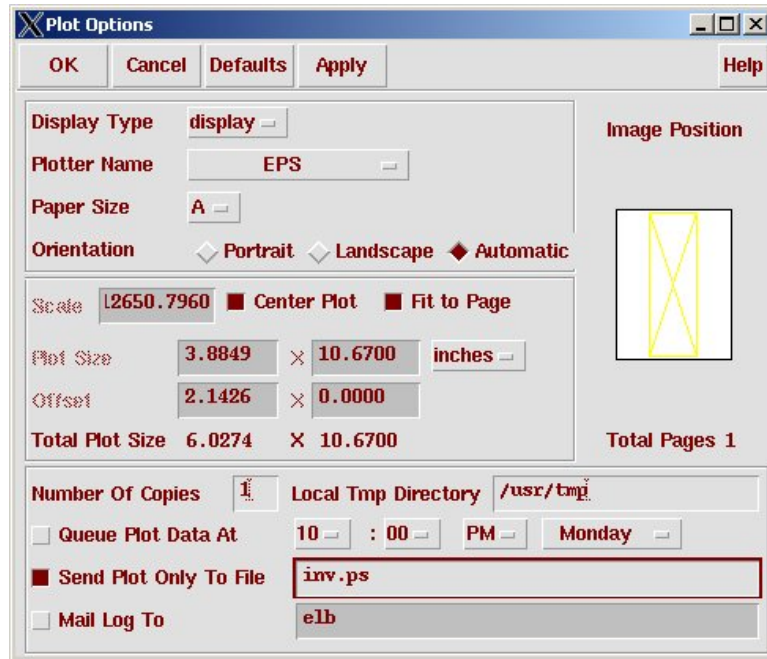
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Figure 5.19: Layout with four inverter instances expanded to see all levels of layout



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Figure 5.20: Submit Plot dialog box



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Figure 5.21: Plot Options dialog box

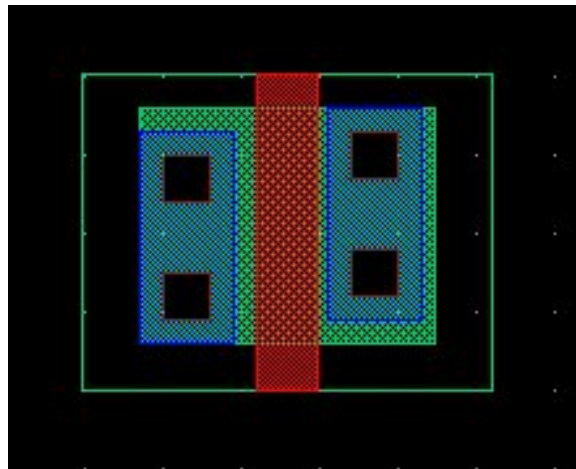
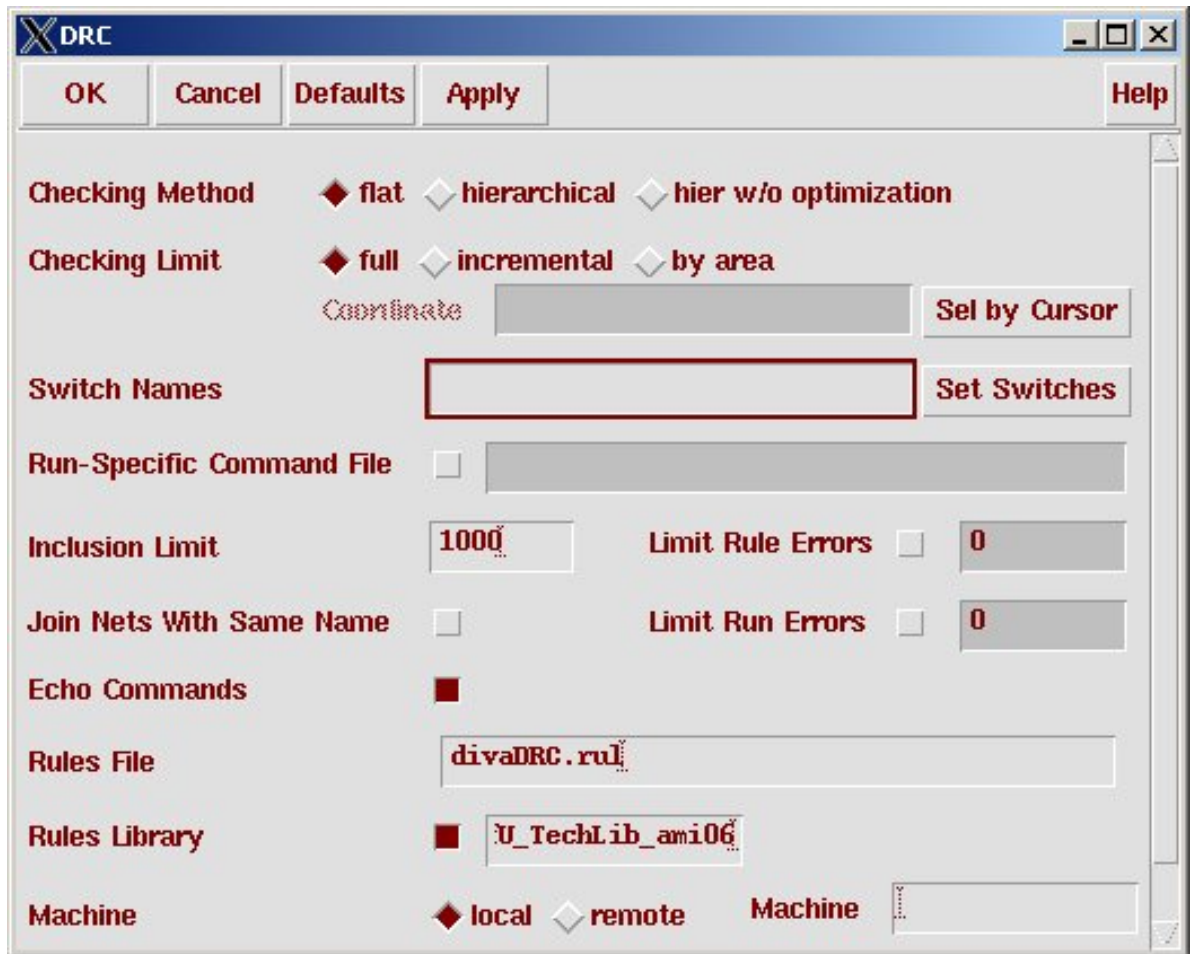
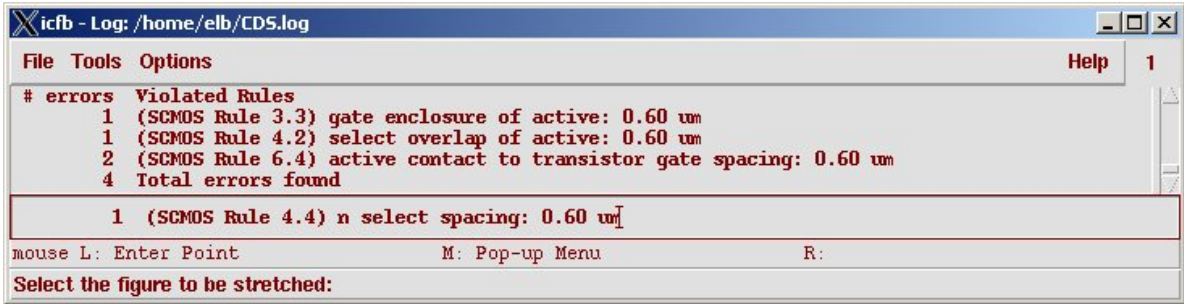


Figure 5.22: Nmos transistor layout (with DRC errors)



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Figure 5.23: DIVA DRC control window



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Figure 5.24: Results from the *DRC* in the *CIW* window

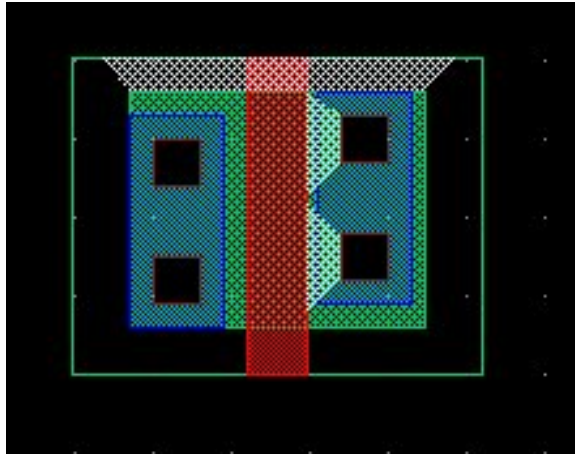
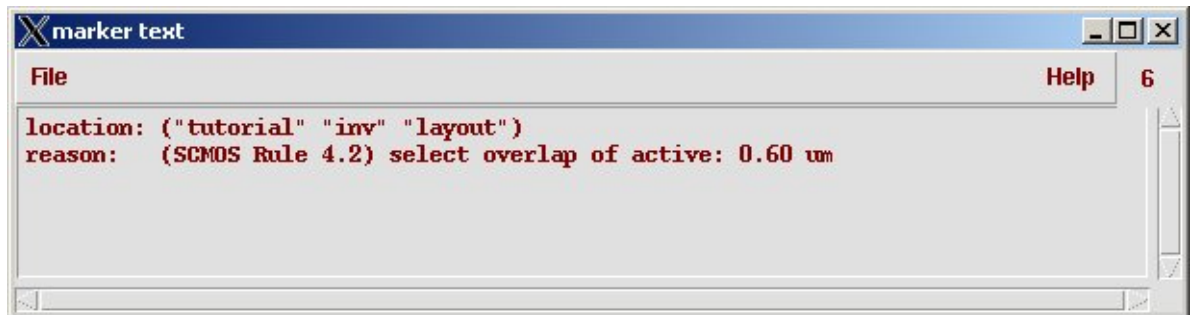
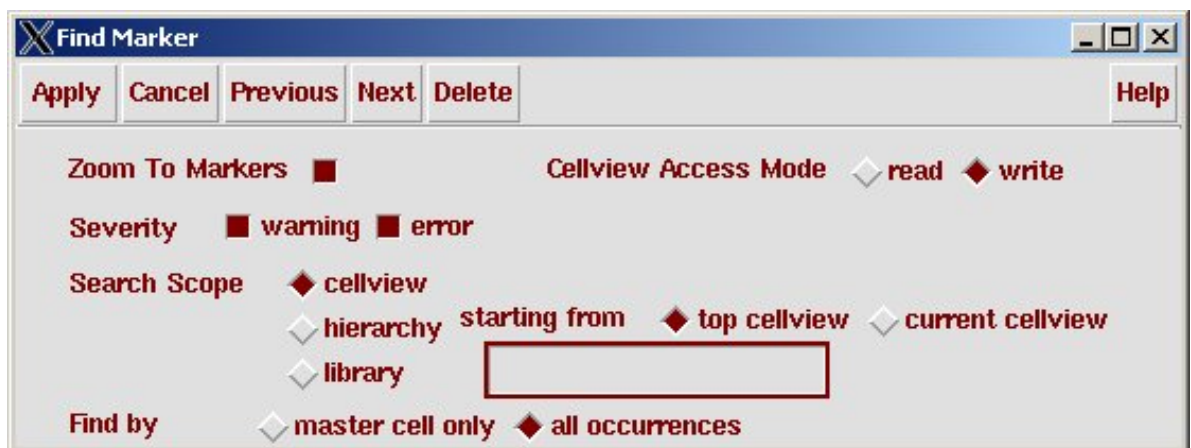


Figure 5.25: Nmos transistor layout (with *DRC* errors flagged)



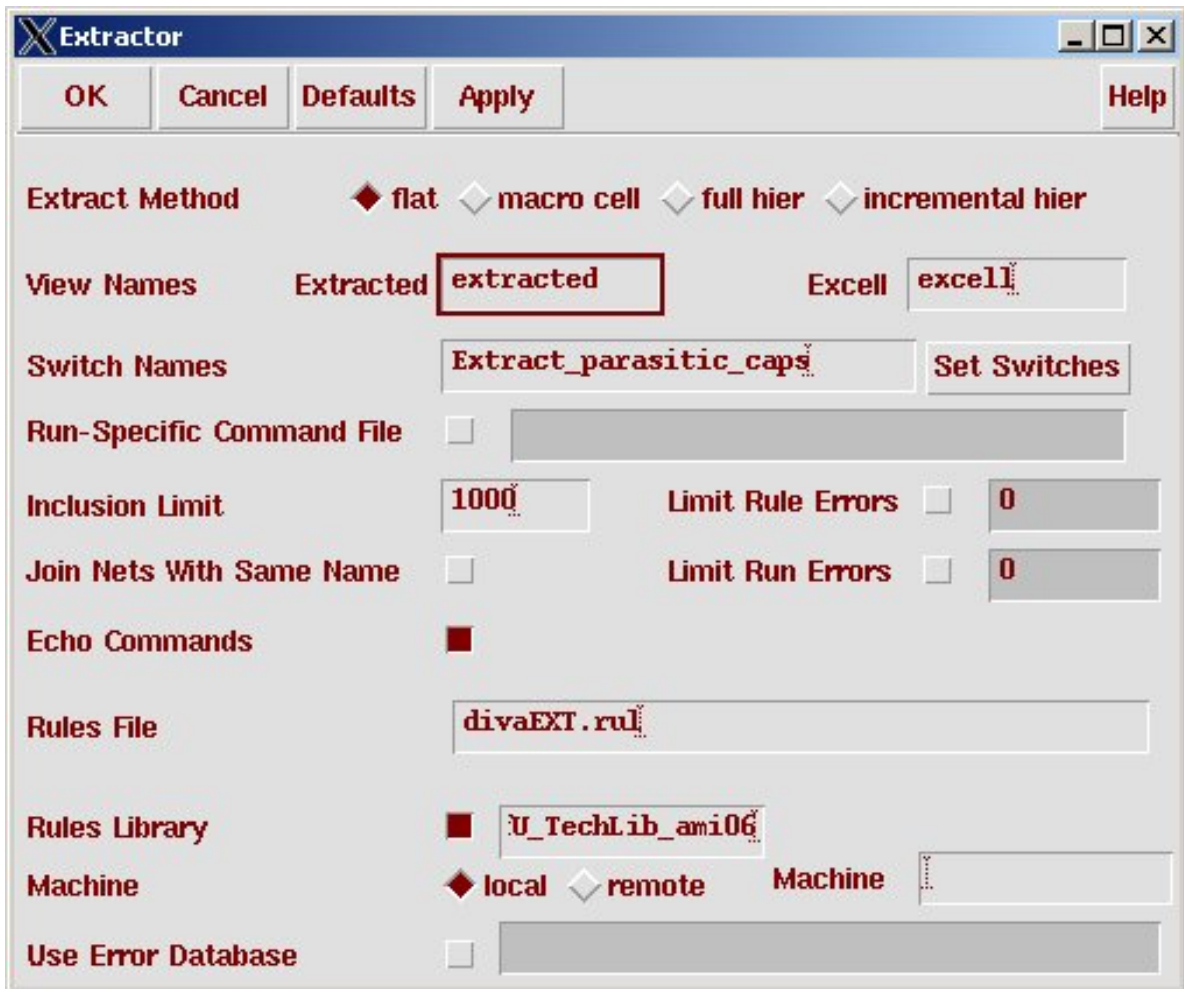
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Figure 5.26: Explanation of *DRC* violation



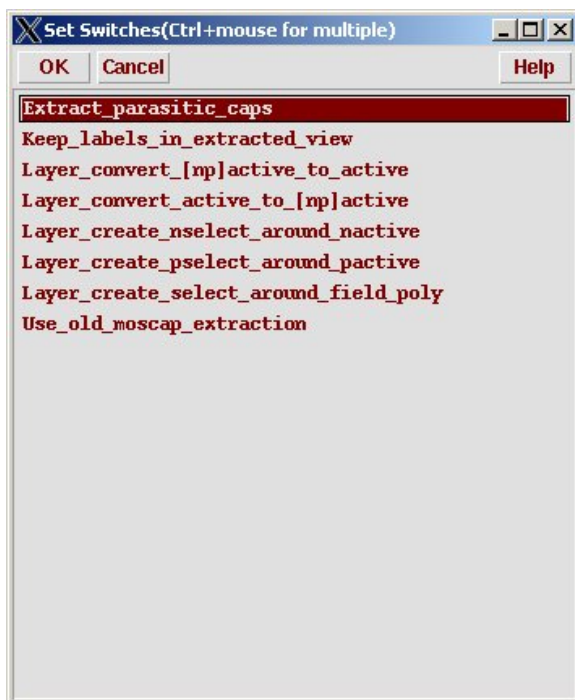
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Figure 5.27: Finding all *DRC* violations



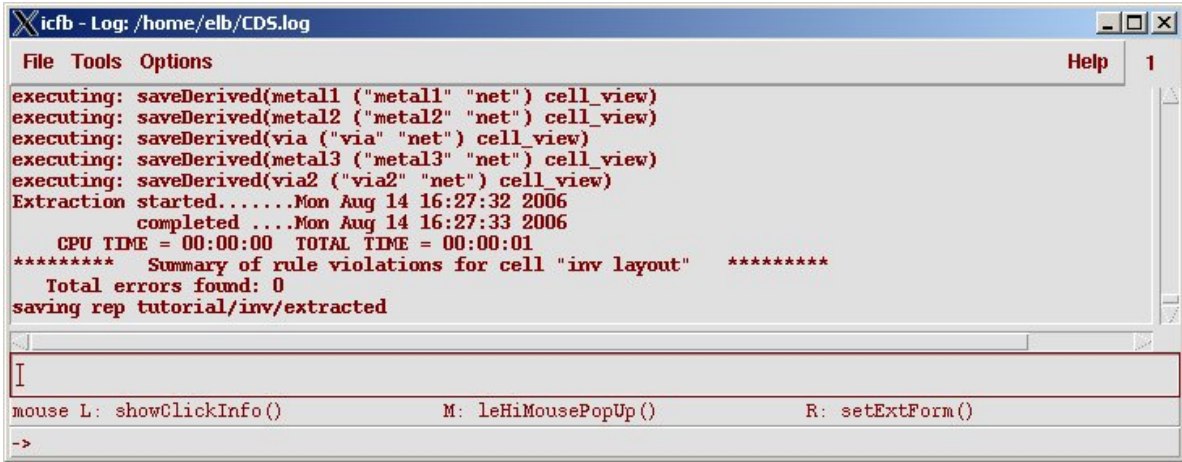
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Figure 5.28: *DIVA* extraction control window



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Figure 5.29: *DIVA* extraction special switches

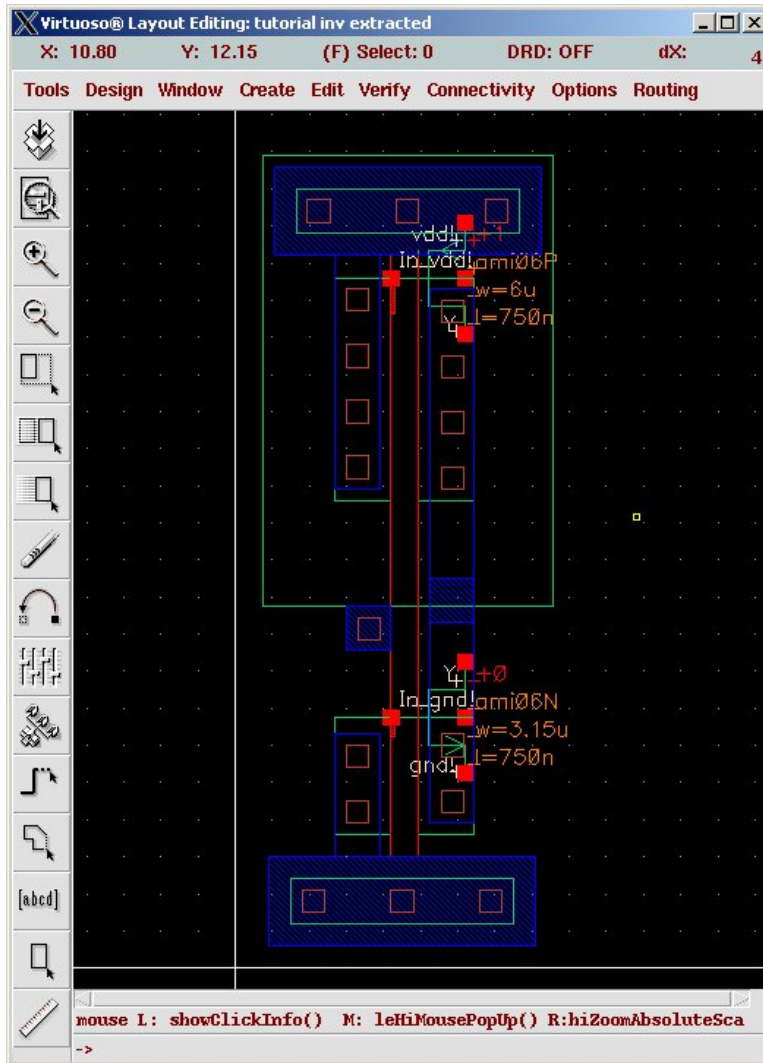


```
icfb - Log: /home/elb/CDS.log
File Tools Options Help 1
executing: saveDerived(metal1 ("metal1" "net") cell_view)
executing: saveDerived(metal2 ("metal2" "net") cell_view)
executing: saveDerived(via ("via" "net") cell_view)
executing: saveDerived(metal3 ("metal3" "net") cell_view)
executing: saveDerived(via2 ("via2" "net") cell_view)
Extraction started.....Mon Aug 14 16:27:32 2006
completed ...Mon Aug 14 16:27:33 2006
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "inv layout" *****
Total errors found: 0
saving rep tutorial/inv/extracted

I
mouse L: showClickInfo() M: leHiMousePopUp() R: setExtForm()
->
```

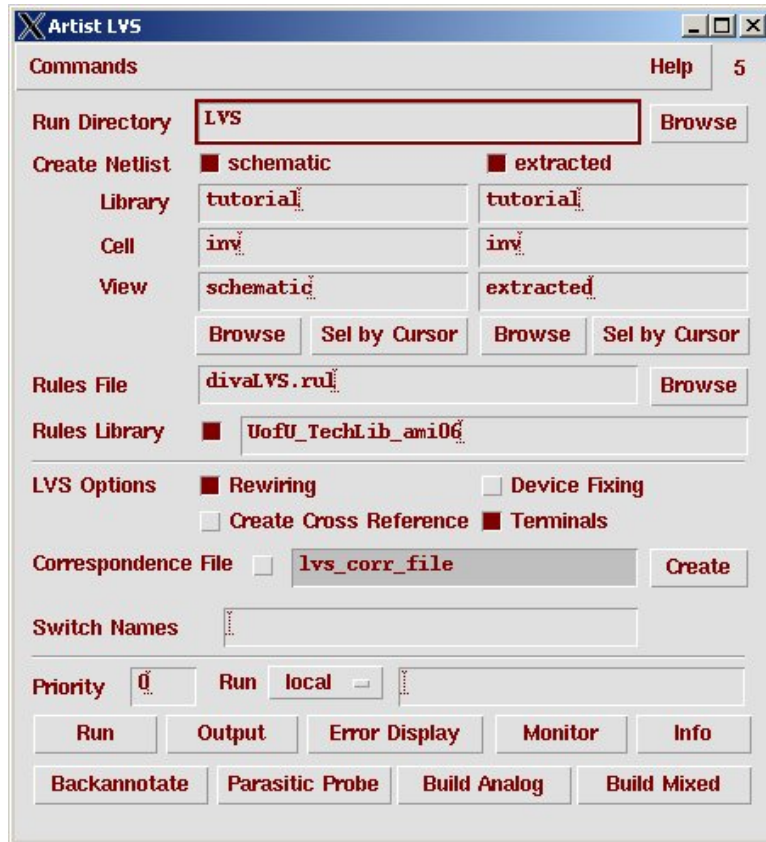
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Figure 5.30: *DIVA* extraction result in the CIW



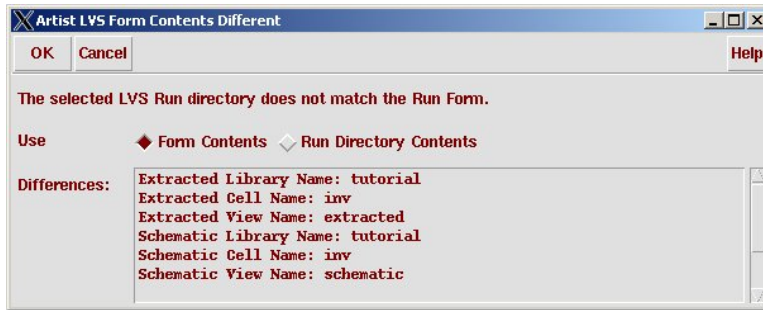
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Figure 5.31: Extracted view of the inverter



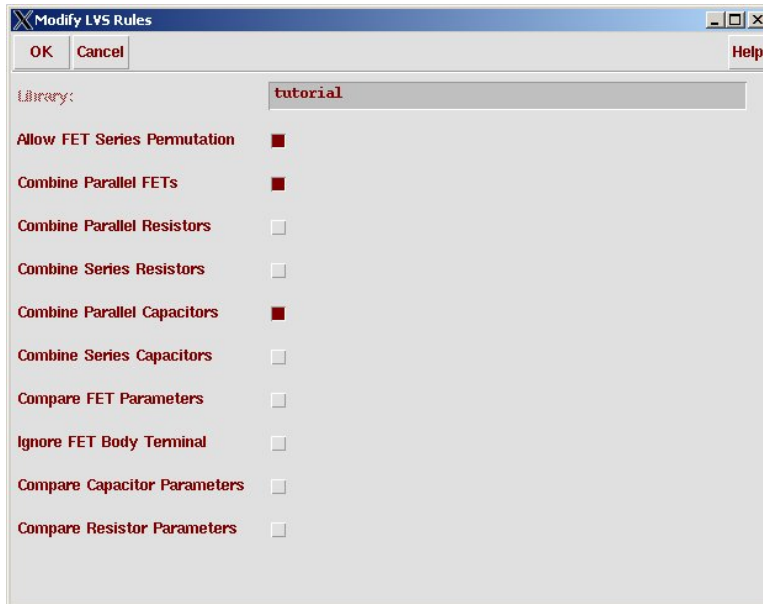
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Figure 5.32: *DIVA* LVS control window



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Figure 5.33: *DIVA* LVS Control Form



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Figure 5.34: NCSU form to modify LVS rules



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Figure 5.35: *DIVA LVS* completion indication

```

/home/elb/IC_CAD/cadencetest/LVS/si.out
File Help 6
@(#)CDS: LVS.exe version 5.1.0 07/23/2006 23:38 (cicln01) $

Command line: /uusoc/facility/cad_tools/Cadence/IC5141ISR200607280110/tools/dfII/bin/
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/elb/IC_CAD/cadencetest/LVS/layout/netlist
count
 4          nets
 4          terminals
 1          pmos
 1          rmos

Net-list summary for /home/elb/IC_CAD/cadencetest/LVS/schematic/netlist
count
 4          nets
 4          terminals
 1          pmos
 1          rmos

Terminal correspondence points
N2      N2      In
N3      N1      gnd!
N1      N0      vdd!

Devices in the rules but not in the netlist:
  cap nfet pfet rmos4 pmos4

The net-lists failed to match.

                layout schematic
                instances
un-matched      0      0
rewired          0      0
size errors     0      0
pruned          0      0
active          2      2
total           2      2

                nets
un-matched      0      0
merged          0      0
pruned          0      0
active          4      4
total           4      4

```

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Figure 5.36: Diva LVS output

```

/home/elb/IC_CAD/cadencetest/LVS/si.out
File Help 6

pruned          0      0
active          4      4
total           4      4

                terminals
un-matched      1      1
matched but
different type   0      0
total           4      4

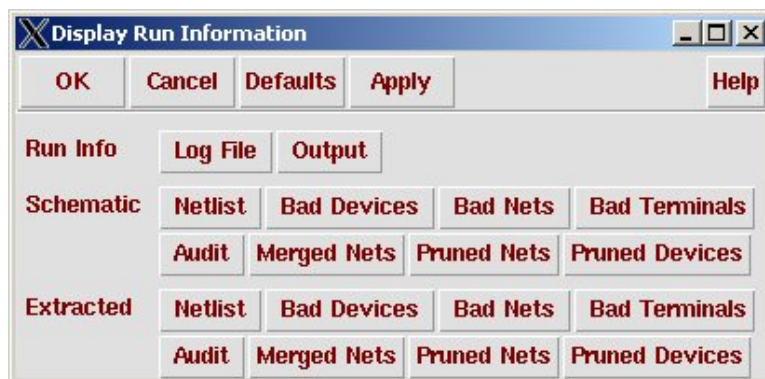
Probe files from /home/elb/IC_CAD/cadencetest/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
T -1 Out /Out
? Terminal Out in the schematic is not present in the layout.
prunenet.out:
prunedev.out:
audit.out:

Probe files from /home/elb/IC_CAD/cadencetest/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
T -1 Y /Y
? Terminal Y in the layout is not present in the schematic.
prunenet.out:
prunedev.out:
audit.out:

```

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Figure 5.37: *DIVA LVS output (scrolled)*



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Figure 5.38: *DIVA LVS* Run Information window

