Verifying a Virtual Component Interface-based PCI Bus Wrapper Using an LSC-Based Specification

Annette Bunker and Ganesh Gopalakrishnan

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School of Computing
University of Utah
Salt Lake City, UT 84112 USA

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Abstract

Because of the high stakes involved in integrating externally developed intellectual property (IP) cores used in System on Chip (SOC) designs, methods and tool support for quick, easy, decisive standard compliance verification must be developed. Such methods and tools include formal standard specifications that are easy to read, formal definitions of standard compliance and automatic generation of model checking assertions which together imply compliance. We compare two efforts in verifying that the same register transfer level (RTL) code complies with the Virtual Sockets Interface Alliance's (VSIA) Virtual Components Interface (VCI) Standard. We show that using Live Sequence Charts (LSCs) as a formal notation for protocol specification has potential to ease the verification effort required.

1 Introduction

As designers rely more and more on externally-developed intellectual property (IP), the necessity of verifying that the IP blocks interface with one another correctly becomes a vital part of the verification task. In an effort to alleviate this concern, the Virtual Socket Interface Alliance VSIA (VSIA) produced the Virtual Component Interface (VCI) Standard. The problem, then, becomes determining whether or not a given IP block correctly implements the VCI standard.

Both the IP designer and the IP integrator face this problem, as the integrator must at least sanity check and possibly fully replicate the verification reported by the developer. Because the same

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