Abstract

We provide a simple formal model for Itanium^{TM} shared memory consistency [1, 2] covering a core set of instructions. Existing descriptions of Itanium shared memory consistency are based on an informal collection of ordering rules as well as several examples. Our operational model employs widely understood data structures such as buffers and memories, and expresses ordering constraints precisely using a collection of nondeterministic rules. This can enable the construction of reliable prototype implementations, formal verification against implementations, formal verification against other formal models, as well as verification of synchronization routines. Our model covers all published ordering constraints, and also sheds light on tricky concepts such as causality.