A Fast Parallel Squarer Based on Divide-and-Conquer

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UUCS-95-011

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August 4, 1995

Abstract

Fast and small squarers are needed in many applications such as image compression. A new family of high performance parallel squarers based on the divide-and-conquer method is reported. Our main result was realizing the basis cases of the divide-and-conquer recursion by using optimized n-bit primitive squarers, where n *is in the range of 2 to 6. This method reduced the gate count and provided shorter critical paths. A chip implementing an 8-bit squarer was designed, fabricated and successfully tested, resulting in 24 MOPS using a 2-μ CMOS fabrication technology. This squarer had two additional features: increased number of squaring operations per unit circuit area, and the potential for reduced power consumption per squaring operation.*