HOP: A Formal Model for Synchronous Circuits using Communicating Fundamental Mode Symbolic Automata*

GANESH GOPALAKRISHNAN (*ganesh@cs.utah.edu*)

University of Utah
Dept. of Computer Science
Salt Lake City, Utah 84112

Keywords: Formal Hardware Specification, Verification, Synchronous VLSI Design, Symbolic Automaton Models

Abstract. We study synchronous digital circuits in an abstract setting. A circuit is viewed as a collection of *modules* connected through their boundary *ports*, where each port assumes a fixed direction (input or output) over one *cycle* of operation, and can change directions across cycles. No distinction is made between clock inputs and non-clock inputs. A cycle of operation consists of the application of a set of inputs followed by the stabilization of the module state before the next inputs are applied (*i.e.* fundamental mode operation is assumed). The states and inputs of a module are modeled *symbolically*, in a functional notation. This enables us to study not only finite-state controllers, but also large data paths, possibly with unbounded amounts of state. We present the abstract syntax for modules, well-formedness checks on the syntax, the formal semantics in terms of the denotation of a module, and the rule for composing two modules interconnected and operating in *parallel*, embodied in the operator *par*. It is shown that *par* preserves well-formedness, and denotes conjunction. These results are applicable to virtually every kind of synchronous circuit (e.g. VLSI circuits that employ single or multiphase clocks, circuits that employ switch or gate logic structures, circuits that employ uni- or bi-directional ports, etc.), thanks to the small number of assumptions upon which the HOP model is set up.